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SEARCH REQUEST FORM

Examiner # (Mandatory): _75667_   Requester's Full Name: _We. Zha_

Art Unit _2762_   Location (Bldg/Room#): _Cryol cPk 2_   Phone (circle 305 306 308) _6437_

Serial Number: _c8/997.142_   Results Format Preferred (circle): PAPER DISK E-MAIL

Title of Invention _method for analyzing capacity of parallel processing system_

Inventors (please provide full names): _Marchal Isma_

Earliest Priority Date: _12/23/1997_

Keywords (include any known synonyms registry numbers, explanation of initialisms):

data graph parallel processing system

execution time , execution performance

counts of data record

amount of data record

Vertices , nodes

parallel processing system

performance monitoring , Load balancing

Search Topic:
Please write detailed statement of the search topic, and the concept of the invention. Describe as specifically as possible the
subject matter to be searched. Define any terms that may have a special meaning. Give examples of relevant citations, authors,
etc., if known. You may include a copy of the abstract and the broadest or most relevant claim(s).

Analyzing the performance and capacity of an application
in a parallel processing system. The application
and system are described as having a graph
representation , data

please see attached claim 1

05-09-20 RUSH

STAFF USE ONLY

Searcher: _____

Searcher Phone #: _318-7795_

Searcher Location: _4B30_

Date Picked Up: _5-10-00_

Date Completed: _5-10-00_

Clerical Prep Time: _30_

Terminal Time: _155_

Number of Databases: _54_

Type of Search	Vendors (include cost where applicable)
___ N.A. Sequence	___ STN
___ A.A. Sequence	___ Questel/Orbit
___ Structure (#)	___ Lexis/Nexis
✓ Bibliographic	✓ WWW/Internet
___ Litigation1	___ In-house sequence systems (list)
___ Fulltext	✓ Dialog _1983 47_
___ Procurement	___ Dr. Link
___ Other	___ Westlaw
	___ Other (specify)

PTO-1590 (2-99)

Cornell Theory Center

Discussion:
Parallel Processing Performance Tools

<u>11/98</u> *Cluck → goes to new dates (see next page)*
(revision history)

This is the in-depth discussion layer of a two-part module. For an explanation of the layers and how to navigate within and between them, return to the <u>top page</u> of this module.

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<u>Lab Exercises</u> ▦ <u>Quiz</u> ▦ <u>Evaluation</u>

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1. Introduction to Optimization

The speed of a message-passing parallel code depends on the performance of both the local hosts and of the message passing environment. Optimization of parallel code is usually carried out in an iterative process involving several tools to investigate performance issues. Many of the computational optimizations are no different from the ones needed for a serial code. For more information, see <u>Performance Basics</u>, <u>Single Processor Performance Tools</u>, <u>Single Processor Performance Considerations for the SP2</u>, and <u>Timing and Optimizing a Fortran Program</u>.

This module will be concerned with issues that range from <u>gathering profile data</u> that will help with the design of a message passing scheme for your application, through <u>debugging</u> the code that you have written, to <u>tracing</u> what actually happened during execution. After each section you will have the option of trying out one or more of the tools that have been discussed.

Overviews of <u>parallel tools</u> at CTC are available under CTC's web site.

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2. Profiling

Author:
John Zollweg
Created: JAZ 12/18/95
Revised: JAZ 10/1/96
Revised: RYL 3/21/97
Revised: JAZ 4/30/98
Revised 9/98 by Sam (Susan A. Martin) to remove back/contents/forward buttons from all but major sections
Revised 9/98 by Sam to standardize layers
Revised 11/98 to add new buttons, etc.

For the purpose of this module, we will define a profiling tool as any tool that reports the cumulative time spent in various parts of a program over the length of a run. A more restrictive definition would limit profilers to tools that obtain timing information by sampling. We will also consider tools that obtain information by embedding timing routines.

Profiling is important in parallel code optimization because the performance of a message passing code is closely related to its *granularity*, defined here as the ratio of the time between communication events to the duration of an event. To minimize time spent communicating, you should maximize your code's granularity by parallelizing at the highest feasible level. Save yourself the trouble of implementing a parallelization strategy that will result in too fine a granularity by discovering from a profiling run that the time T between message passing events is quite short. A good rule of thumb is that T should be greater than ten times the latency for sending a message.

For HPF codes, profilers should also be used in conjunction with compiler parallelization reports to determine the effect of adding HPF directives to your code. You need to determine whether you've coded correctly, and whether the compiler is handling the directives as you expected.

Tool	Description	Source	Status
Xprofiler	Subroutines and statements, Any code compiled with IBM XL compilers	IBM prototype	Working, Comm. not accurately attributed
Forge Profiling	HPF subroutines and loops, Breakdown of communication overhead	APR	Working
Pgprof	HPF subroutines and statements, Per process or summarized	Portland Group	Working
Time Functions	Greatest control, Any code	Varies	Working

Exercise   Try Pgprof

Table of Contents   1   2   3   4   Less Detail

3. Debugging

To debug a message-passing code, you can use IBM's parallel debugger or a serial debugger (if you are not running very many processes). All provide the standard serial debugging actions. All require the -g flag at compile time, to associate the source code you wrote with the assembly language code.

You cannot use these debuggers directly on HPF code since, at some stage, the compiler translates the code to message-passing. If your compiler allows the intermediate message-passing code to be saved, and you are desperate, it is possible to use a debugger on this code. The generated code is usually not very readable, variables are often renamed, and loop indices re-formulated.

Tool	Description	Source	Status
Pdbx/Pedb	Command-line or graphical interface, One or multiple windows, Parallel task manipulation	IBM PE	Working
Xldb	Serial debugger, Graphical interface, One window per task	IBM XL compilers	Working
Dbx	Serial debugger, Command line interface, One session per task, Can diagnose deadlock	UNIX	Working

[Exercise] Try Pedb   [Exercise] Try Pdbx   [Exercise] Try Xldb

[Table of Contents] [1] [2] [3] [4] [Less Detail]

4. Tracing

It is from a trace that you usually get the most information about how well your parallel job is doing. Here that you can find out exactly when tasks stall because they are waiting for messages. Tracing involves (at least) two steps: generating the trace and viewing the results.

At runtime, trace records are written when message-passing library routines are called or at set time intervals. The trace records contain the type of event and a timestamp. After the run completes, you can use a tool to graphically display and summarize this data.

All the tools listed below have full functionality on message-passing programs. NTV, Vampir, VT, and Pablo will also work for HPF programs. To use source association (the tool's ability to point to the location in the source code where a trace record was generated) on a HPF code with NTV and VT, the program must be compiled with xlhpf or xlhpf90.

Tool	Description	Source	Status
NTV	Static timeline for complete run, Communication summaries, Source association, Easy to use/learn	NASA	Working
Vampir	Static or animated displays, Timeline, node usage, information on messages, Smaller trace files	Pallas GmbH	Working
VT	Many communication and system displays, Animated displays, Source association on current event	IBM PE	Working
UTE Nupshot	Timeline, function summaries, efficiency, Minimum overhead for trace generation, Source association, Follow other AIX events	IBM, Argonne Nat'l Lab	Not Working
Pablo	Can construct trace analysis routines, Many different message-passing libraries	University of Illinois	Working

Exercise Try NTV   **Exercise** Try Vampir   **Exercise** Try VT

Exercise Pablo Tutorial 1   **Exercise** Pablo Tutorial 2

4.1 Converting Trace File Formats

Each of the trace display tools requires that the trace file be in a different format. VT requires .trc, nupshot needs .ups, and Pablo wants .sddf. If you have done your own profiling (see below), you may have a trace file in alog format. Fortunately, there are three translators available for making conversions.

alog2ups converts files from alog (old upshot format) into .ups (nupshot format).

mp2sddf converts files from VT format (.trc) into SDDF format.

ute2sddf converts files from UTE format (.ups) into SDDF format.

An additional advantage of the SDDF format is that it is ASCII text, so it can be browsed with an editor if you are trying to track down a tracing problem or want to see a specific event record.

4.2 Profiling Combined with Tracing

Profilers and tracing tools "instrument" your code for you. If you don't feel that these are displaying the information you are most interested in, in the most usable form, you could consider adding your own profiling calls to your program.

Tool	Description	Source	Status
Vampir	MPI code, Can show duration of state	Pallas GmbH	Working
NTV/VT	MPI/MPL code, Can show location of event	IBM PE	Working
Alog/Nupshot	Any message passing library, Can show duration of state	Argonne Nat'l Lab	Not working
UTE Markers	MPI code, Can show duration of state	IBM	Not working

Table of Contents   **1**   **2**   **3**   **4**   **Less Detail**

Quiz Take a multiple-choice quiz on this material, and submit it for grading.

Exercise Access all profiling, debugging, and tracing exercises.

Evaluation Please complete this short evaluation form. Thank you!

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URL http://www.tc.cornell.edu/Edu/Talks/Performance/ParallelPerfTools/more.html

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Discussion:
Parallel Processing Performance Tools: VT

<u>Back to module</u>

VT

Using VT

<u>VT</u> is the portion of the IBM Parallel Environment devoted to trace visualization and performance monitoring. The *IBM Parallel Environment for AIX: Operation and Use Version 2.1.0 manual (GC23-3891-00)* devotes 80 pages to VT. Thus, only a few of the highlights are mentioned here.

A VT trace file is produced by specifying a nonzero value for the environment variable `MP_TRACELEVEL`. Recognized values and their consequences are:

```
1      Markers only

2      Markers and kernel statistics

3      Markers, messages, collective communication

9      Everything
```

The trace file is automatically named by appending `.trc` to the name of the executable.

Trace files contain a lot of information, so they tend to grow very rapidly. If message passing traffic is high, trace files can be as large as 0.1 MB/node/second. To limit the amount of trace information, you may insert calls to routines `VT_TRC_START(level,error)` and `VT_TRC_STOP(error)` in your code. Also, care must be taken that both the temporary and merged trace files are written in directories with sufficient space. It is best to set `MP_TMPDIR=/tmp/scratch/<username>` and, for a batch job, use `MP_TRACEDIR=/sptmp/trace` .

To view a trace file (*a.out*.trc) that you have already produced, invoke VT with `vt -tfile a.out.trc`. You will get a view selection window that gives you many options. If you traced everything (MP_TRACELEVEL=9 when you collected the trace), then both system and user events will be available for viewing.

VT Screen Dumps

Best Available Copy
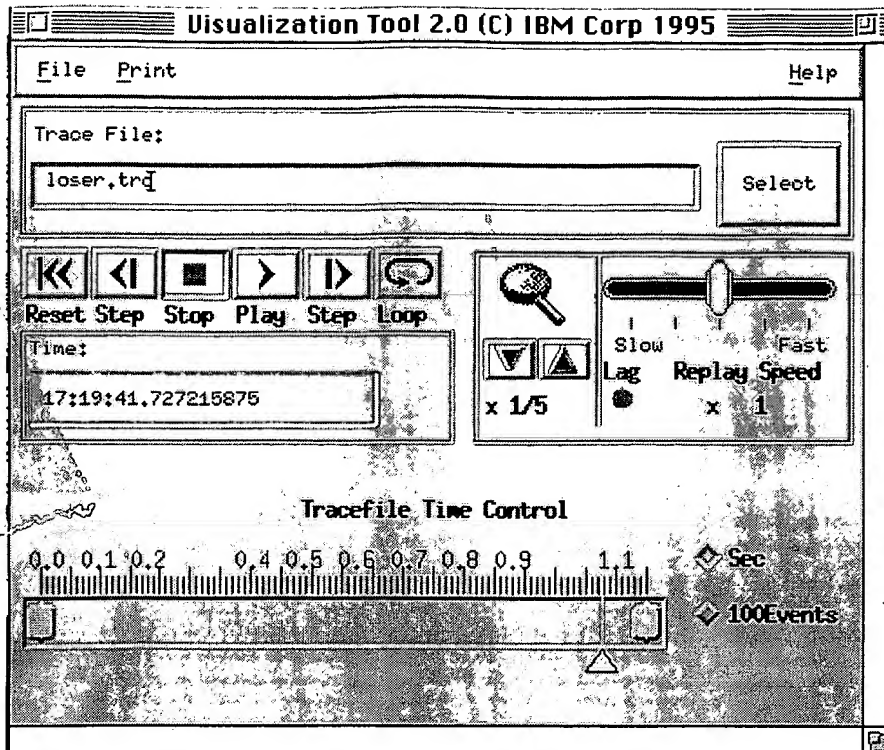
This is the VT control panel. Most VT views are animated; VT attempts to draw them at the same speed that the original program ran. Some are instantaneous (you only view the current state); some are streaming (the past state is left on the display). The controls allow the program to be run continuously or stepped-through (note the VCR-like buttons), the view to be magnified, and start and endpoints for playback to be selected.
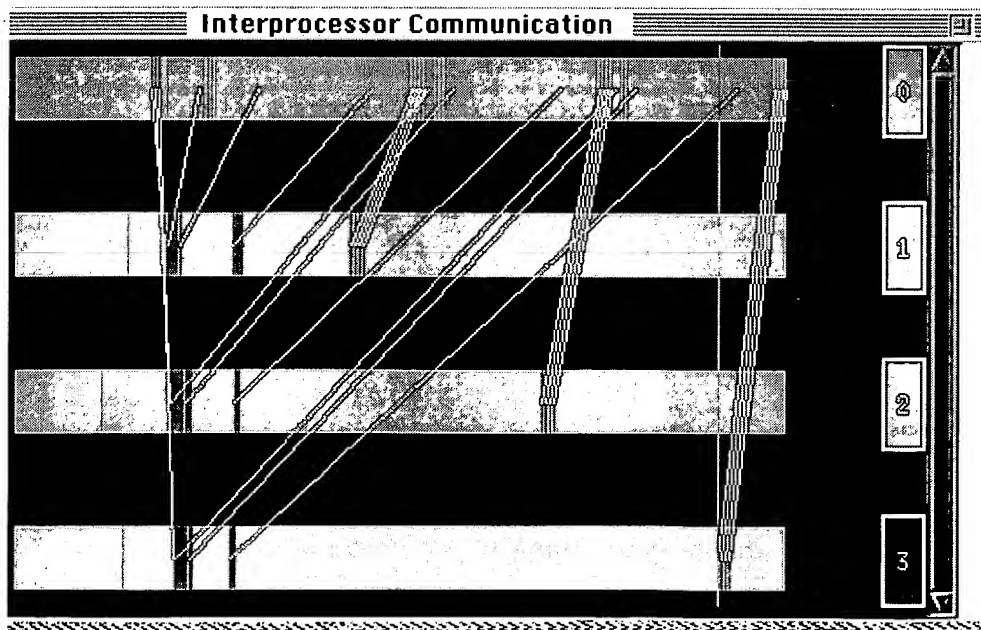
The user can select any number of views of the trace information, although the playback will slow down considerably if many views are opened. This is the "Interprocessor Communication" display, a color-coded timeline that shows what message-passing state (if any) each task was in. Arrows are drawn for communication events. You can use a search menu to locate where an event of interest occurred.

If you left-click on the "Interprocessor Communication" display, a popup window gives the time and the

state the task was in. The time scale for the display is not labeled. It is also not uniform unless the colored bars are solid. Bars that are shown hatched are not as long as they should be, given the magnification chosen.
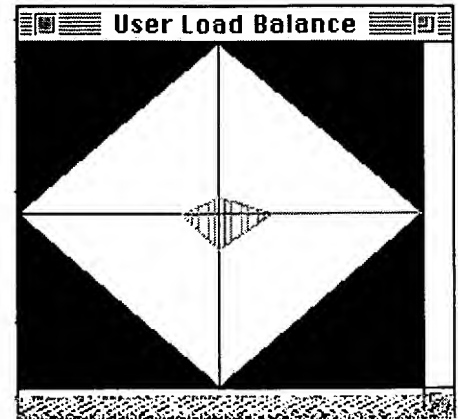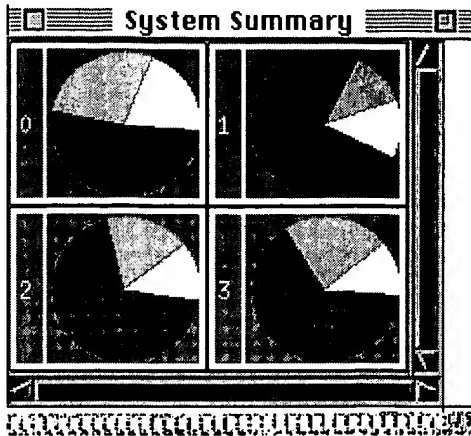
The "System Summary" display shows the amount of processor time spent running the program (in green), running the operating system (in blue), waiting for resources (in yellow), and idle (none shown here). Usage is averaged over a very short interval by default. If you want to see it averaged over the trace up to the current event, right-click in the display and select show cumulative.

The "User Load Balance" display shows the instantaneous and average cpu percentage for the program. Instantaneous is 0 (all yellow) in this example, but the hashed green polygon indicates the average cpu percentage.

Back to module

```
?show files;ds
File 348:European Patents 1978-2000/Apr W03
        (c) 2000 European Patent Office
File 349:PCT Fulltext 1983-2000/UB=, UT=20000413
        (c) 2000 WIPO/MicroPatent

Set    Items   Description
S1        0    PN=AU 662842 + PN=AU 8779120 + PN=AU 8930887 + PN=AU 91884-
               57 + PN=AU 9349160 + PN=AU 9917909 + PN=BR 8703308 + PN=CA 12-
               38434 + PN=CA 1263729 + PN=CA 1304824 + PN=CA 1310428 + PN=CA
               1321654 + PN=CA 2008902 + PN=CA 2017835
S2        0    PN=CA 2044313 + PN=CA 2068580 + PN=CA 2186688 + PN=DE 3587-
               668 + PN=DE 3607241 + PN=DE 3685599 + PN=DE 3789175 + PN=DE 3-
               853257 + PN=DE 3853336 + PN=DE 3854035 + PN=DE 3855234 + PN=DE
               3889557 + PN=DE 3909153 + PN=DE 3924759
S3       10    PN=DE 68928311 + PN=DE 68928980 + PN=DE 69131122 + PN=DE 6-
               9322057 + PN=DE 69418646 + PN=EP 146250 + PN=EP 160848 + PN=EP
```

7 May 10, 2000 10:32

```
              195589 + PN=EP 235764 + PN=EP 254854 + PN=EP 279227 + PN=EP -
              313788 + PN=EP 314341 + PN=EP 314909 + PN=EP 315647
S4       15    PN=EP 329771 + PN=EP 358292 + PN=EP 388806 + PN=EP 425174 +
              PN=EP 428327 + PN=EP 429733 + PN=EP 461608 + PN=EP 474747 + -
              PN=EP 490624 + PN=EP 501025 + PN=EP 524683 + PN=EP 595453 + P-
              N=EP 604341 + PN=EP 627682 + PN=EP 631252
S5        2    PN=EP 773649 + PN=EP 843257 + PN=GB 2231985 + PN=GB 2262175
              + PN=JP 10011421 + PN=JP 10031615 + PN=JP 10031755 + PN=JP 1-
              0055350 + PN=JP 10161884 + PN=JP 1076272 + PN=JP 1194032 + PN-
              =JP 2500393 + PN=JP 2779713 + PN=JP 2968060
S6        0    PN=JP 3026984 + PN=JP 3501176 + PN=JP 4113473 + PN=JP 4211-
              858 + PN=JP 4260149 + PN=JP 4505678 + PN=JP 5012232 + PN=JP 5-
              039698 + PN=JP 6121353 + PN=JP 61214694 + PN=JP 6161973 + PN=-
              JP 62172461 + PN=JP 6237270 + PN=JP 7200508
S7        0    PN=JP 7253954 + PN=JP 8077128 + PN=JP 8123852 + PN=JP 8171-
              537 + PN=JP 8212186 + PN=JP 8293873 + PN=JP 9034850 + PN=JP 9-
              091261 + PN=JP 9212339 + PN=JP 9223123 + PN=JP 9244825 + PN=JP
              9266476 + PN=JP 9282290 + PN=KR 98010819
S8        0    PN=SE 511098 + PN=SE 9704565 + PN=SU 1388882 + PN=SU 14050-
              70 + PN=US 34528 + PN=US 36444 + PN=US 4646075 + PN=US 4649498
              + PN=US 4752777 + PN=US 4780821 + PN=US 4814762 + PN=US 4814-
              978 + PN=US 4816814 + PN=US 4829451 + PN=US 4866637
S9        0    PN=US 4928247 + PN=US 4943556 + PN=US 5020059 + PN=US 5097-
              411 + PN=US 5111389 + PN=US 5146568 + PN=US 5155822 + PN=US 5-
              191651 + PN=US 5193188 + PN=US 5200915 + PN=US 5249274 + PN=US
              5251322 + PN=US 5271014 + PN=US 5280627
S10       0    PN=US 5317682 + PN=US 5327570 + PN=US 5333279 + PN=US 5367-
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              5517654 + PN=US 5566342 + PN=US 5587922
S11       2    PN=US 5590356 + PN=US 5592405 + PN=US 5606520 + PN=US 5696-
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              5940086 + PN=US 6041398 + PN=WO 8800732
S12       7    PN=WO 8901664 + PN=WO 9015390 + PN=WO 9208196 + PN=WO 9930-
              456 + PN=ZA 9306275
S13      33    S1:S12
S14   12419    (PARALLEL OR PIPELINE OR ARRAY OR VECTOR OR CONCURRENT? OR
              SIMULTANEOUS?)(2N)(PROCESSOR? ? OR PROCESSING OR SERVER)
S15    2619    HYPERCUBE? ? OR HYPER()CUBE? ? OR SMP OR MPP
S16       0    MC=(T01-M02C? OR T01-F03B?)
S17    1565    IC=G06F-015/16
S18  381974    CAPACITY OR PERFORMANCE OR LOAD OR EXECUT?(2N)TIME? ? OR R-
              ESOURCE? ? OR THROUGHPUT OR THROUGH()PUT OR TRAFFIC OR CONCUR-
              RENCY OR BOTTLENECK? ? OR TRACE()TOOL? ? OR STATISTIC? ? OR W-
              ORKLOAD OR CLUSTER(2N)MANAG? OR DATA()HANDLING
S19  602621    GRAPH? OR VISUAL? OR PICTORIAL OR PICTURE OR 3()D OR THREE-
              ()DIMENSIONAL OR 3D OR IMAGE OR IMAGES OR ILLUSTRATION OR X()Y
              OR XY OR MATRIX OR MATRICES
S20  127453    NODE OR NODES OR VERTEX OR VERTICES OR CORNER OR TRIANGULAR
              OR TRIANGLE? ? OR CROSS()POINT? ? OR CROSSPOINT? ? OR FORK? ?
S21   14723    S14 OR S15
S22    2058    S18(S)S19(S)S20
S23      82    S21(S)S22
S24      61    S17 AND S22
S25     126    S23:S24
S26      61    S17 AND S25
S27      30    S13 NOT S26
S28       0    S27 AND PR=19980101:20000510
?t27/5/all
```

27/5/1   (Item 1 from file: 348)

DIALOG(R)File 348:European Patents
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01062005
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348 ,
**COMMUNICATION SYSTEM AND METHOD OF SENDING MESSAGES IN A COMMUNICATION
    SYSTEM**
**SYSTEME DE COMMUNICATIONS ET PROCEDE D'ENVOI DE MESSAGES DANS UN SYSTEME DE
    COMMUNICATIONS**
PATENT ASSIGNEE:
  Telefonaktiebolaget L M Ericsson (Publ), (213764), , 126 25 Stockholm,
    (SE), (Applicant designated States: all)
INVENTOR:
  VASELL, Jesper, Sten Sturegatan 4, S-411 39 Goteborg, (SE)
PATENT (CC, No, Kind, Date):
                              WO 9930456 990617
APPLICATION (CC, No, Date):   WO 98962746 981130; WO 98SE2177 981130
PRIORITY (CC, No, Date): SE 974565 971208
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI;
  LU; MC; NL; PT; SE
INTERNATIONAL PATENT CLASS: H04L-001/00
LEGAL STATUS (Type, Pub Date, Kind, Text):
 Application: 990818 A2 International application. (Art. 158(1))
 Application: 990818 A2 International application entering European
                           phase
LANGUAGE (Publication,Procedural,Application): English; English; English

 27/5/2   (Item 2 from file: 348)
DIALOG(R)File 348:European Patents
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00924915
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
Improved code optimiser for pipelined computers
Code-Optimierer fur Pipeline-Rechner
Optimiseur de code pour des ordinateurs a pipeline
PATENT ASSIGNEE:
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    Mountain View, California 94043-1100, (US), (applicant designated
    states: AT;BE;CH;DE;DK;ES;FI;FR;GB;GR;IE;IT;LI;LU;MC;NL;PT;SE)
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  Beylin, Boris, 771 Ames Avenue, Palo Alto, CA 94303, (US)
  Subramanian, Krishna, 20990 Valley Green, No.630 Cupertino, CA 95014,
    (US)
LEGAL REPRESENTATIVE:
  Leeming, John Gerard (74731), J.A. Kemp & Co., 14 South Square, Gray's
    Inn, London WC1R 5LX, (GB)
PATENT (CC, No, Kind, Date): EP 843257 A2 980520 (Basic)
                             EP 843257 A3 990519
APPLICATION (CC, No, Date):   EP 97309064 971111;
PRIORITY (CC, No, Date): US 752683 961119
DESIGNATED STATES: DE; FR; GB; NL; SE
INTERNATIONAL PATENT CLASS: G06F-009/45;

ABSTRACT EP 843257 A2
    Apparatus and methods are disclosed to provide improved optimizations
  of single-basic-block-loops. These optimizations include improved
  scheduling of blocking instructions for pipelined computers and improved
  scheduling and allocation of resources (such as registers) that cannot be
  spilled to memory. Scheduling of blocking instructions is improved by
  pre-allocating space in the scheduling reservation table. Improved

scheduling and allocation of non-spillable resources results from
converting the resource constraint into a data dependency constraint.
ABSTRACT WORD COUNT: 71

LEGAL STATUS (Type, Pub Date, Kind, Text):
 Examination: 20000105 A2 Date of request for examination: 19991108
 Application: 980520 A2 Published application (A1with Search Report
                            ;A2without Search Report)
 Search Report: 990519 A3 Separate publication of the European or
                            International search report
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language   Update   Word Count
      CLAIMS A (English) 9821   733
      SPEC A   (English) 9821   6840
Total word count - document A   7573
Total word count - document B   0
Total word count - documents A + B   7573

  27/5/3   (Item 3 from file: 348)
DIALOG(R)File 348:European Patents
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00835461
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
Network topology management system
Netzwerk - Topologie-Verwaltungssystem
Systeme de gestion pour topologie de reseau
PATENT ASSIGNEE:
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    California 94043-1100, (US), (applicant designated states:
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LEGAL REPRESENTATIVE:
  O'Connell, David Christopher (62551), Haseltine Lake & Co., Imperial
    House, 15-19 Kingsway, London WC2B 6UD, (GB)
PATENT (CC, No, Kind, Date): EP 773649 A2 970514 (Basic)
APPLICATION (CC, No, Date):   EP 96307993 961105;
PRIORITY (CC, No, Date): US 558274 951113
DESIGNATED STATES: DE; FR; GB; IT; NL; SE
INTERNATIONAL PATENT CLASS: H04L-012/24;

ABSTRACT EP 773649 A2
    A system and method for maintaining complex relationships between
  computer network elements provides a common database for storing node,
  type, and view data. The views are created and maintained by the network
  management system. When a new node is added or parentage of a node is
  changed, the views of a node are modified in a network database.
ABSTRACT WORD COUNT: 59

LEGAL STATUS (Type, Pub Date, Kind, Text):
 Application: 970514 A2 Published application (A1with Search Report
                            ;A2without Search Report)
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language   Update   Word Count
      CLAIMS A (English) EPAB97   712
      SPEC A   (English) EPAB97   3037

Total word count - document A   3749
Total word count - document B   0
Total word count - documents A + B   3749

 27/5/4   (Item 4 from file: 348)
DIALOG(R)File 348:European Patents
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00656035
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
**Draw processor for a high performance three dimensional graphics
   accelerator.**
**Zeichnungsverarbeitungsgerat   fur   drei-dimensionalen   graphischen
   Hoch-Leistungsbeschleuniger.**
**Processeur de dessin pour accelerateur graphique tridimensionnel a haute
   performance.**
PATENT ASSIGNEE:
   SUN MICROSYSTEMS, INC., (1392732), 2550 Garcia Avenue, Mountain View,
      California 94043-1100, (US), (applicant designated states: DE;GB;NL)
INVENTOR:
   Deering, Michael F., 657 Cuesta Drive, Los Altos, California 94024, (US)
LEGAL REPRESENTATIVE:
   Wombwell, Francis (46021), Potts, Kerr & Co. 15, Hamilton Square,
      Birkenhead Merseyside L41 6BR, (GB)
PATENT (CC, No, Kind, Date): EP 631252 A2 941228 (Basic)
                              EP 631252 A3 950315
APPLICATION (CC, No, Date):   EP 94302543 940411;
PRIORITY (CC, No, Date): US 82065 930623
DESIGNATED STATES: DE; GB; NL
INTERNATIONAL PATENT CLASS: G06F-015/72;

ABSTRACT EP 631252 A2
   A draw processor for a graphics accelerator is disclosed that performs
   edgewalking and scan interpolation functions to render a three
   dimensional geometry object defined by a draw packet. The draw processor
   renders a subset of pixels on a scan line, such that a set draw
   processors taken together render the entire geometry object. The draw
   processor renders pixels into an interleave bank of a multiple bank
   interleaved frame buffer. The draw processor also processes direct port
   data through a direct port pipeline . (see image in original document)
ABSTRACT WORD COUNT: 90

LEGAL STATUS (Type, Pub Date, Kind, Text):
 Application: 941228 A2 Published application (A1with Search Report
                            ;A2without Search Report)
 Search Report: 950315 A3 Separate publication of the European or
                            International search report
 Examination: 950628 A2 Date of filing of request for examination:
                            950501
 Examination: 990113 A2 Date of despatch of first examination report:
                            981126
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language   Update   Word Count
      CLAIMS A (English)   EPABF2   825
      SPEC A   (English)   EPABF2   11023
Total word count - document A   11848
Total word count - document B   0
Total word count - documents A + B   11848

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27/5/5   (Item 5 from file: 348)
DIALOG(R)File 348:European Patents
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00651529
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
Floating-point processor for a high performance three dimensional graphics accelerator
Gleitkommaprozessor   fur   einen   hochleistungsfahigen   dreidimensionalen Graphikbeschleuniger
Processeur   a   virgule   flottante   pour   un   accelerateur   graphique tri-dimensionnel a haute performance
PATENT ASSIGNEE:
  SUN MICROSYSTEMS, INC., (1392732), 2550 Garcia Avenue, Mountain View,
    California 94043-1100, (US), (applicant designated states: DE;FR;GB;NL)
INVENTOR:
  Deering, Michael F., 657 Cuesta Drive, Los Altos, California 94024, (US)
LEGAL REPRESENTATIVE:
  Wombwell, Francis (46021), Potts, Kerr & Co. 15, Hamilton Square,
    Birkenhead Merseyside L41 6BR, (GB)
PATENT (CC, No, Kind, Date): EP 627682 A1 941207 (Basic)
                              EP 627682 B1 990526
APPLICATION (CC, No, Date):   EP 94302534 940411;
PRIORITY (CC, No, Date): US 71709 930604
DESIGNATED STATES: DE; FR; GB; NL
INTERNATIONAL PATENT CLASS: G06F-009/38; G06T-015/00;

ABSTRACT EP 627682 A1
    A floating-point processor for a high performance three dimensional
    graphics accelerator in a computer system is disclosed. The
    floating-point processor implements specialized graphics micro
    instructions. The specialized graphics micro instructions include a swap
    micro instruction which causes a hardware remapping of general purpose
    register groups to sort triangle vertices. The specialized graphics micro
    instructions also include specialized conditional branches for three
    dimensional geometry. (see image in original document)
ABSTRACT WORD COUNT: 70

LEGAL STATUS (Type, Pub Date, Kind, Text):
 Application: 941207 A1 Published application (A1with Search Report
                            ;A2without Search Report)
 Examination: 950628 A1 Date of filing of request for examination:
                            950501
 Examination: 980121 A1 Date of despatch of first examination report:
                            971205
 Change: 990317 A1 International patent classification (change)
 Change: 990317 A1 Obligatory supplementary classification
                            (change)
 Grant: 990526 B1 Granted patent
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9921	1439
CLAIMS B	(German)	9921	1195
CLAIMS B	(French)	9921	1749
SPEC B	(English)	9921	7619
Total word count - document A			0
Total word count - document B			12002
Total word count - documents A + B			12002

27/5/6   (Item 6 from file: 348)

12 May 10, 2000 10:32

DIALOG(R)File 348:European Patents
(c) 2000 European Patent Office. All rts. reserv.

00605943
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
A parallel scalable internetworking unit architecture.
Parallele, skalierbare Architektur einer internetzwerkenden Einheit.
Architecture parallele et echelonnee pour une unite de communication
    interreseau.
PATENT ASSIGNEE:
  International Business Machines Corporation, (200120), Old Orchard Road,
    Armonk, N.Y. 10504, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
  Yang, Michael Shih, R.D. 2 Laura Lane, Katonah, NY 10536, (US)
  Yih, Jih-Shyr, 2474 Trelawn Street, Yorkstown Heights, NY 10598, (US)
LEGAL REPRESENTATIVE:
  Lattard, Nicole (16571), Compagnie IBM France Departement de Propriete
    Intellectuelle, F-06610 La Gaude, (FR)
PATENT (CC, No, Kind, Date): EP 604341 A2 940629 (Basic)
                              EP 604341 A3 960207
APPLICATION (CC, No, Date):   EP 93480178 931104;
PRIORITY (CC, No, Date): US 996384 921223
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: H04L-029/06;

ABSTRACT EP 604341 A2
    An parallel scalable internetworking unit (IWU) architecture employing
    at least two network controllers (PMI), a foreground buffer controller
    (FGAM) with local memory, a background buffer controller (BGAM) with
    local memory, a node processor (NP) and a buffer memory. Each network
    attached to the IWU has an individual PMI which communicates with the
    FGAM. The FGAM interfaces with PMIs and maintains queueing information.
    The BGAM communicates with the FGAM for maintaining packets of data as
    linked lists of buffers in the buffer memory. The NP communicates with
    both the FGAM and the BGAM to process stored header information. And, a
    connection matrix is provided to dynamically interconnect multiple IWUs
    for increased parallel processing of packet traffic and processing. (see
    image in original document)
ABSTRACT WORD COUNT: 140

LEGAL STATUS (Type, Pub Date, Kind, Text):
 Application: 940629 A2 Published application (A1with Search Report
                            ;A2without Search Report)
 Examination: 941214 A2 Date of filing of request for examination:
                            941021
 Search Report: 960207 A3 Separate publication of the European or
                            International search report
 Withdrawal: 961218 A2 Date on which the European patent application
                            was withdrawn: 961015
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language   Update   Word Count
     CLAIMS A (English)   EPABF2   877
     SPEC A   (English)   EPABF2   5552
Total word count - document A   6429
Total word count - document B   0
Total word count - documents A + B   6429

 27/5/7   (Item 7 from file: 348)
DIALOG(R)File 348:European Patents
(c) 2000 European Patent Office. All rts. reserv.

13 May 10, 2000 10:32

00600490
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
Distributed data processing system
Verteiltes Datenverarbeitungssystem
Systeme de traitement de donnees distribue
PATENT ASSIGNEE:
  INTERNATIONAL COMPUTERS LIMITED, (233330), ICL House, Putney, London,
    SW15 1SW, (GB), (applicant designated states: DE;FR;GB)
INVENTOR:
  Van Den Berg, Thomas Wilhelmus, 11 Hyde Fold Close, Bibby Lane, Burnage,
    Manchester M19 1EN, (GB)
LEGAL REPRESENTATIVE:
  Guyatt, Derek Charles et al (31321), Intellectual Property Department
    International Computers Limited Cavendish Road, Stevenage, Herts, SG1
    2DY, (GB)
PATENT (CC, No, Kind, Date): EP 595453 A1 940504 (Basic)
                                         EP 595453 B1 981111
APPLICATION (CC, No, Date):   EP 93306677 930823;
PRIORITY (CC, No, Date): GB 9222390 921024; GB 9308877 930429
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G06F-009/46; G06F-011/14;
CITED REFERENCES (EP A):
  8TH INT. CONF. ON DISTRIBUTED COMPUTING SYSTEMS 13 June 1988 , IEEE
    COMP.SOC.PRESS, WASHINGTON, USA pages 224 - 233 XP10791 MARINA ROESLER
    ET AL. 'Efficient deadlock resolution for lock-based concurrency
    control schemes'
  21ST INT. SYMP. ON FAULT-TOLERANT COMPUTING 25 June 1991 , IEEE
    COMP.SOC.PRESS, LOS ALAMITOS, USA , XP242728 ERHARD RAHM 'Recovery
    concepts for data sharing systems'
  17TH INT. SYMP. ON FAULT-TOLERANT COMPUTING 6 July 1987 , IEEE
    COMP.SOC.PRESS, LOS ALAMITOS, USA pages 14 - 19 DAVID B. JOHNSON ET AL.
    'Sender-based message logging'
  OPERATING SYSTEMS REVIEW (SIGOPS). vol. 24, no. 1 , January 1990 , NEW
    YORK US pages 27 - 39 XP140327 \ZALP BABAOGLU 'Fault-tolerant computing
    based on mach';

ABSTRACT EP 595453 A1
    A distributed data processing system includes a distributed resource
  manager which detects dependencies between transactions caused by
  conflicting lock requests. A distributed transaction manager stores a
  wait-for graph with nodes representing transactions and edges the nodes
  and representing dependencies between the transactions. Each edge is
  labelled with the identities of the lock requests that caused the
  dependency. The distributed transaction manager propagates probes through
  the wait-for graph, to detect cyclic dependencies, indicating deadlock. A
  deadlock message is then sent to the resource manager identifying a
  particular lock request as a victim for detection to resolve the
  deadlock. (see image in original document)
ABSTRACT WORD COUNT: 104

LEGAL STATUS (Type, Pub Date, Kind, Text):
 Application: 940504 A1 Published application (A1with Search Report
                          ;A2without Search Report)
 Examination: 941123 A1 Date of filing of request for examination:
                          940923
 Examination: 971210 A1 Date of despatch of first examination report:
                          971022
 Grant: 981111 B1 Granted patent
 Oppn None: 991103 B1 No opposition filed: 19990812
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

14 May 10, 2000 10:32

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Available Text   Language    Update    Word Count
     CLAIMS B   (English)   9846         500
     CLAIMS B   (German)    9846         500
     CLAIMS B   (French)    9846         618
     SPEC B     (English)   9846        8178
Total word count - document A             0
Total word count - document B          9796
Total word count - documents A + B     9796
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27/5/8   (Item 8 from file: 348)
DIALOG(R)File 348:European Patents
(c) 2000 European Patent Office. All rts. reserv.

00534022
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
Scientific visualization system.
Wissenschaftliches Anzeigesystem.
Systeme de visualisation scientifique.
PATENT ASSIGNEE:
  INTERNATIONAL BUSINESS MACHINES CORPORATION, (200125), Old Orchard Road,
    Armonk, N.Y. 10504, (US), (applicant designated states: DE;FR;GB;IT)
INVENTOR:
  Carcia, Armando, 2821 Larkspur Street, Yorktown Heights, New York 10598,
    (US)
  Foster, David James, 25 Rockledge Avenue, White Plains, New York 10601,
    (US)
  Pearson, Robert Bernard, RD 1, Box 209N, Beale Road, Cold Spring, New
    York 10516, (US)
LEGAL REPRESENTATIVE:
  Jost, Ottokarl, Dipl.-Ing. (6092), IBM Deutschland GmbH Patentwesen und
    Urheberrecht Schonaicher Strasse 220, W-7030 Boblingen, (DE)
PATENT (CC, No, Kind, Date): EP 524683 A1 930127 (Basic)
APPLICATION (CC, No, Date):   EP 92202126 920711;
PRIORITY (CC, No, Date): US 734432 910722
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: G06F-013/40;
CITED PATENTS (EP A): EP 379768 A; EP 369265 A

ABSTRACT EP 524683 A1
   A multiprocessor data processing system (10), and a method of operating
same, so as to provide efficient bandwidth utilization of shared system
resources (24, 26). The system includes a plurality of processor nodes,
each of which includes a data processor (22a, 28a). In accordance with a
method of the invention a first step buffers data written by a data
processor to a first bus (23a), prior to the data being transmitted to a
second bus (32). A second step also buffers byte enable (BE) signals
generated by the data processor in conjunction with the data written by
the data processor. A third step performs a main memory (26) write
operation by the steps of: transmitting the buffered data to the second
bus; responsive to the stored BE signals, also transmitting a control
signal for indicating if a memory write is to be accomplished as a
read-modify-write (RMW) type of memory operation; and transmitting the
stored BE signals to the second bus. A further step couples the data, the
RMW signal, and the BE signals from the local bus to a third bus (24) for
reception by the main memory. Interface circuitry (34) associated with
the main memory is responsive to the RMW signal for (a) reading data from
a specified location within the main memory, (b) selectively merging the
transmitted data in accordance with the BE signals, and (c) storing the
previously read and merged data back into the specified location. (see
image in original document)
ABSTRACT WORD COUNT: 248

LEGAL STATUS (Type, Pub Date, Kind, Text):
 Application: 930127 A1 Published application (A1with Search Report
                              ;A2without Search Report)
 Examination: 930714 A1 Date of filing of request for examination:
                              930519
 Examination: 960501 A1 Date of despatch of first examination report:
                              960319
*Assignee: 970205 A1 Applicant (transfer of rights) (change):
                              International Business Machines Corporation
                              (200120) Old Orchard Road Armonk, N.Y. 10504
                              (US) (applicant designated states: DE;FR;GB;IT)
 Withdrawal: 970326 A1 Date on which the European patent application
                              was deemed to be withdrawn: 961001
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language   Update   Word Count
      CLAIMS A (English) EPABF1   1969
      SPEC A   (English) EPABF1   14967
Total word count - document A   16936
Total word count - document B   0
Total word count - documents A + B   16936

 27/5/9   (Item 9 from file: 348)
DIALOG(R)File 348:European Patents
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00474959
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
**Centralized and distributed wait depth limited concurrency control methods
    and apparatus.**
**Zentralisiertes und verteiltes Gleichzeitigkeitssteuerungsverfahren und
    Gerat mit Beschrankung der Wartetiefe.**
**Procede et dispositif centralise et distribue de commande de simultaneite
    avec limitation de profondeur.**
PATENT ASSIGNEE:
  International Business Machines Corporation, (200120), Old Orchard Road,
    Armonk, N.Y. 10504, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
  Franaszek, Peter A., P.O. Box 704, Yorktown Heights, New York 10598, (US)
  Robinson, John Timothy, 3314 North Deerfield Avenue, Yorktown Heights,
    New York 10598, (US)
  Thomasian, Alexander, 17 Meadowbrook Road, Pleasantville, New York 10570,
    (US)
LEGAL REPRESENTATIVE:
  Schafer, Wolfgang, Dipl.-Ing. (62021), European Patent Attorney, IBM
    Deutschland GmbH, Schonaicher Strasse 220, W-7030 Boblingen, (DE)
PATENT (CC, No, Kind, Date): EP 501025 A2 920902 (Basic)
                              EP 501025 A3 921230
APPLICATION (CC, No, Date):   EP 91121110 911209;
PRIORITY (CC, No, Date): US 660762 910225
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G06F-015/403;
CITED REFERENCES (EP A):
  PROCEEDINGS OF THE ELEVENTH ANNUAL INTERNATIONAL COMPUTER SOFTWARE &
    APPLICATIONS CONFERENCE 9 October 1987, TOKYO, JAPAN pages 554 - 560
    YAHIKO KAMBAYASHI, XINGGUO ZHONG 'CONTROLLABLE TIMESTAMP ORDERING AND
    ORIENTAL TIMESTAMP ORDERING CONCURRENCY CONTROL MECHANISMS'
  PROCEEDINGS OF THE MINI AND MICROCOMPUTERS AND THEIR APPLICATIONS
    CONFERENCE 30 June 1988, SANT FELIU DE GUIXOLS, SPAIN pages 197 - 201
    SONG C. MOON, YOO S. KIM 'A HYBRID CONCURRENCY CONTROL SCHEME IN

                    16 May 10, 2000 10:32

DISTRIBUTED DATABASE SYSTEMS';

ABSTRACT EP 501025 A2
    A wait depth limited concurrency control method for use in a multi-user
data processing environment restricts the depth of the waiting tree to a
predetermined depth, taking into account the progress made by
transactions in conflict resolution. In the preferred embodiment for a
centralized transaction processing system, the waiting depth is limited
to one. Transaction specific information represented by a real-valued
function L, where for each transaction T in the system at any instant in
time $L(T)$ provides a measure of the current "length" of the transaction,
is used to determine which transaction is to be restarted in case of a
conflict between transactions resulting in a wait tree depth exceeding
the predetermined depth. $L(T)$ may be the number of locks currently held
by a transaction T, the maximum of the number of locks held by any
incarnation of transaction T, including the current one, or the sum of
the number of locks held by each incarnation of transaction T up to the
current one. In a distributed transaction processing system, $L(T)$ is
based on time wherein each global transaction is assigned a starting
time, and this starting time is included in the startup message for each
subtransaction, so that the starting time of global transaction is
locally known at any node executing one of its subtransactions. (see
image in original document)
ABSTRACT WORD COUNT: 224

LEGAL STATUS (Type, Pub Date, Kind, Text):
 Application: 920902 A2 Published application (A1with Search Report
                             ;A2without Search Report)
 Search Report: 921230 A3 Separate publication of the European or
                             International search report
 Examination: 930203 A2 Date of filing of request for examination:
                             921210
 Withdrawal: 970226 A2 Date on which the European patent application
                             was withdrawn: 961223
LANGUAGE (Publication,Procedural,Application): English; English; English

 27/5/10   (Item 10 from file: 348)
DIALOG(R)File 348:European Patents
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00463691
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
Device for rapidly solving a symmetric linear system on a supercomputer.
Vorrichtung zur   schnellen Losung eines linearen symmetrischen Systems in
    einem Superrechnersystem.
Dispositif resolvant rapidement un systeme lineaire symetrique sur un
    superordinateur.
PATENT ASSIGNEE:
  NEC CORPORATION, (236690), 7-1, Shiba 5-chome Minato-ku, Tokyo 108-01,
    (JP), (applicant designated states: DE;FR;GB)
INVENTOR:
  Hayami, Ken, c/o NEC Corporation, 7-1, Shiba 5-chome, Minato-ku, Tokyo,
    (JP)
  Watanabe, Hiroshi, c/o NEC Scientific Information, System Development,
    Ltd., 100-1, Sakado, Takatsu-ku, Kawasaki-shi, Kanagawa, (JP)
LEGAL REPRESENTATIVE:
  Vossius & Partner (100311), Siebertstrasse 4 P.O. Box 86 07 67, W-8000
    Munchen 86, (DE)
PATENT (CC, No, Kind, Date): EP 461608 A2 911218 (Basic)
                              EP 461608 A3 940518
APPLICATION (CC, No, Date):   EP 91109544 910611;

PRIORITY (CC, No, Date): JP 90151664 900612
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G06F-015/347; G06F-015/328; G06F-015/324;
CITED REFERENCES (EP A):
  INTERNATIONAL JOURNAL OF SUPERCOMPUTER APPLICATIONS vol. 1, no. 1 , 1987
    , CAMBRIDGE, MA US pages 70 - 98 XP000099181 RAMI MELHEM ET AL 'TOWARD
    EFFICIENT IMPLEMENTATION OF PRECONDITIONED CONJUGATE GRADIENT METHODS
    ON VECTOR SUPERCOMPUTERS'
  PARALLEL COMPUTING vol. 9, no. 1 , December 1988 , AMSTERDAM NL pages 359
    - 365 ILIO GALLIANI ET AL 'SOLVING LARGE SYSTEMS OF LINEAR ORDINARY
    DIFFERENTIAL EQUATIONS ON A VECTOR COMPUTER'
  PROCCEDINGS OF THE 1988 INTERNATIONAL CONFERENCE ON PARALLEL PROCESSING,
    THE PENN STATE UNIVERSITY PRESS, PENNSYLVANIA, US 15 August 1988 ,
    UNIVERSITY PARK, PENNSYLVANIA, US pages 32 - 38 XP000042203 P.S.TSENG
    'ITERATIVE SPARSE LINEAR SYSTEM SOLVERS ON WARP'
  PARALLEL COMPUTING vol. 11, no. 2 , August 1989 , AMSTERDAM NL pages 223
    - 239 XP000047175 G.RADICATI ET AL 'PARALLEL CONJUGATE GRADIENT-LIKE
    ALGORITHMS FOR SOLVING SPARSE NONSYMMETRIC LINEAR SYSTEMS ON A VECTOR
    MULTIPROCESSOR'
  MATHEMATICS AND COMPUTERS IN SIMULATION, NORTH HOLLAND PUBLISHING COMPANY
    vol. 21 , 1979 , AMSTERDAM, NL pages 368 - 375 D.R.KINCAID ET AL 'THE
    USE OF ITERATIVE METHODS FOR SOLVING LARGE SPARSE PDE-RELATED LINEAR
    SYSTEMS'
  COMPUTER PHYSICS COMMUNICATIONS, NORTH HOLLAND vol. 53 , 1989 ,
    AMSTERDAM, NL pages 283 - 293 T.C.OPPE ET AL 'AN OVERVIEW OF NSPCG: A
    NONSYMMETRIC PRECONDITIONED CONJUGATE GRADIENT PACKAGE';

ABSTRACT EP 461608 A2
    In order to solve a symmetric linear system given by Au = b, where A
represents a symmetric coefficient matrix equal to a three-term sum of a
diagonal matrix plus an upper triangular matrix plus a lower triangular
matrix, b represents a right-hand side vector, and u represents a
solution vector, a device calculates the solution vector by using the
right-hand side vector, the diagonal matrix, and the upper triangular
matrix. Supplied with an array (JA) representing a column number of the
upper triangular matrix, a pointer array constructing section (11)
constructs a pointer array (JL) which points to the lower triangular
matrix. Supplied with an array (AA) and the array (JA) which collectively
represent a combination of the diagonal matrix and the upper triangular
matrix, a matrix decomposing section (12) decomposes the array (AA) into
an approximate matrix (M) which approximates the symmetric coefficient
matrix. A first product calculating section (16) calculates a first
product vector (y) by using the array (AA), the array (JA), a first
vector (x), and the pointer array (JL). A second product calculating
section (17) calculates a second product vector (y') by using the
approximate matrix (M) and the second vector (x'). An iterative
calculating section (18) carries out iterative calculation on the array
(AA), the array (JA), an array (B) representing the right-hand side
vector, the first and the second product vectors (y) and (y'). The
iterative calculating section (18) iteratively provides the first and the
second product calculating sections (16) and (17) with the first and the
second vectors (x) and (x'), respectively. The iterative calculating
section (18) produces the solution vector (u). The device may be supplied
with the lower triangular matrix instead of the upper triangular matrix.
    (see image in original document)
ABSTRACT WORD COUNT: 295

LEGAL STATUS (Type, Pub Date, Kind, Text):
 Application: 911218 A2 Published application (A1with Search Report
                     ;A2without Search Report)
 Examination: 911218 A2 Date of filing of request for examination:
                     910710

Change: 940511 A2 Obligatory supplementary classification
                               (change)
Search Report: 940518 A3 Separate publication of the European or
                               International search report
Examination: 960403 A2 Date of despatch of first examination report:
                               960216
Withdrawal: 981202 A2 Date on which the European patent application
                               was deemed to be withdrawn: 980609
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language   Update   Word Count
      CLAIMS A (English)   EPABF1   714
      SPEC A   (English)   EPABF1   4993
Total word count - document A   5707
Total word count - document B   0
Total word count - documents A + B   5707

27/5/11   (Item 11 from file: 348)
DIALOG(R)File 348:European Patents
(c) 2000 European Patent Office. All rts. reserv.

00448936
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
**PARALLEL   DISTRIBUTED   PROCESSING   NETWORK   CHARACTERIZED BY AN INFORMATION
    STORAGE MATRIX.**
**PARALLEL   VERTEILTES   VERARBEITUNGSNETZWERK   GEKENNZEICHNET   DURCH   EINE
    INFORMATIONSSPEICHERMATRIX.**
**RESEAU   DE   TRAITEMENT REPARTI PARALLELEMENT ET CARACTERISE PAR UNE MATRICE
    DE STOCKAGE D'INFORMATIONS.**
PATENT ASSIGNEE:
  E.I. DU PONT DE NEMOURS AND COMPANY, (200580), 1007 Market Street,
    Wilmington Delaware 19898, (US), (applicant designated states:
    AT;BE;CH;DE;DK;ES;FR;GB;IT;LI;LU;NL;SE)
INVENTOR:
  SAMARDZIJA, Nikola, 138 Belmont Drive, Wilmington, DE 19808, (US)
LEGAL REPRESENTATIVE:
  Davies, Christopher Robert et al (53231), Frank B. Dehn & Co. Imperial
    House 15-19 Kingsway, London WC2B 6UZ, (GB)
PATENT (CC, No, Kind, Date): EP 474747 A1   920318 (Basic)
                              EP 474747 A1   930602
                              WO 9015390   901213
APPLICATION (CC, No, Date):   EP 90909020 900521; WO 90US2699 900521
PRIORITY (CC, No, Date): US 360804 890602
DESIGNATED STATES: AT; BE; CH; DE; DK; ES; FR; GB; IT; LI; LU; NL; SE
INTERNATIONAL PATENT CLASS: G06F-015/18;
CITED PATENTS (WO A): US 4752906 A; US 4809193 A; US 4731747 A
CITED REFERENCES (EP A):
  AIP CONFERENCE PROCEEDINGS 151 : NEURAL NETWORKS FOR COMPUTING 1986,
    SNOWBIRD , USA pages 386 - 391 SASIELA 'Forgetting as a way to improve
    neural-net behavior'
  IEEE FIRST INTERNATIONAL CONFERENCE ON NEURAL NETWORKS vol. 3, 21 June
    1987, SAN DIEGO , USA pages 191 - 198 SOMANI 'Compact neural network';
NOTE:
  No A-document published by EPO
LEGAL STATUS (Type, Pub Date, Kind, Text):
  Application: 920318 A1 Published application (A1with Search Report
                             ;A2without Search Report)
  Examination: 920318 A1 Date of filing of request for examination:
                             911224
  Search Report: 930602 A1 Drawing up of a supplementary European search
                             report: 930415

19 May 10, 2000 10:32

Withdrawal: 930915 A1 Date on which the European patent application
                              was withdrawn: 930630
LANGUAGE (Publication,Procedural,Application): English; English; English

27/5/12   (Item 12 from file: 348)
DIALOG(R)File 348:European Patents
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00436196
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
Processor array system.
Feldrechnersystem.
Systeme de processeurs en reseau.
PATENT ASSIGNEE:
  AMT(HOLDINGS) LIMITED, (1014030), 65 Suttons Park Avenue, Reading
    Berkshire RG6 1AZ, (GB), (applicant designated states:
    AT;BE;CH;DE;DK;ES;FR;GB;GR;IT;LI;LU;NL;SE)
INVENTOR:
  Hunt, David John, 3 Moores Green, Wokingham, Berkshire, RG11 1QG, (GB)
LEGAL REPRESENTATIVE:
  Rackham, Stephen Neil et al (35061), GILL JENNINGS & EVERY 53-64 Chancery
    Lane, London WC2A 1HN, (GB)
PATENT (CC, No, Kind, Date): EP 428327 A1 910522 (Basic)
APPLICATION (CC, No, Date):   EP 90312204 901108;
PRIORITY (CC, No, Date): GB 8925721 891114
DESIGNATED STATES: AT; BE; CH; DE; DK; ES; FR; GB; GR; IT; LI; LU; NL; SE
INTERNATIONAL PATENT CLASS: G06F-015/80;
CITED PATENTS (EP A): EP 191280 A; US 4144566 A
ABSTRACT EP 428327 A1
    A processor array employs an SIMD architecture and includes a number of
  sub-arrays (S1...S4). Each sub-array (S1...S4) includes n processor
  elements (PE). Each processor element is connected to local store
  including on-chip memory. Each sub-array is connected to a region of
  off-chip memory by an m-bit wide path, where m is an integer greater than
  1. The m-bit wide path is selectively configurable as a one-bit path to
  or from each of m processor elements or as an m-bit wide path arranged to
  communicate complete m-bit words of memory data between the region of
  off-chip memory and respective processor elements.
ABSTRACT WORD COUNT: 104

LEGAL STATUS (Type, Pub Date, Kind, Text):
  Application: 910522 A1 Published application (A1with Search Report
                              ;A2without Search Report)
  Examination: 920102 A1 Date of filing of request for examination:
                              911108
  Examination: 940720 A1 Date of despatch of first examination report:
                              940606
  Withdrawal: 950412 A1 Date on which the European patent application
                              was deemed to be withdrawn: 941018
LANGUAGE (Publication,Procedural,Application): English; English; English

27/5/13   (Item 13 from file: 348)
DIALOG(R)File 348:European Patents
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00435370
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
Parametric curve evaluation for a computer graphics display system.
Parametrische Kurvenabschatzung fur graphisches Anzeigesystem mit Rechner.
Evaluation de courbe parametrique pour systeme d'affichage graphique a

calculateur.
PATENT ASSIGNEE:
  International Business Machines Corporation, (200120), Old Orchard Road,
    Armonk, N.Y. 10504, (US), (applicant designated states: DE;FR;GB;IT)
INVENTOR:
  Luken, William Louis, Jr., 2 Orchard Hill Road, Ulster Park, New York
    12487, (US)
LEGAL REPRESENTATIVE:
  Blakemore, Frederick Norman et al (28381), IBM United Kingdom Limited
    Intellectual Property Department Hursley Park, Winchester Hampshire
    SO21 2JN, (GB)
PATENT (CC, No, Kind, Date): EP 425174 A2 910502 (Basic)
                              EP 425174 A3 921007
APPLICATION (CC, No, Date):   EP 90311369 901017;
PRIORITY (CC, No, Date): US 426912 891024
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: G06F-015/353;
CITED PATENTS (EP A): EP 277832 A; EP 314335 A; US 4760548 A
CITED REFERENCES (EP A):
  COMPUTER AIDED DESIGN vol. 19, no. 9, November 1987, LONDON pages 485 -
    498; L. PIEGL ET AL.: 'CURVE AND SURFACE CONSTRUCTIONS USING RATIONAL
    B-SPLINES';

ABSTRACT EP 425174 A2
    A method and apparatus are described for evaluating and rendering
  parametric curves. The apparatus includes a system memory connected to a
  pipelined arrangement of a graphics control processor, a plurality of
  parallel floating point processors, another floating point processor, a
  clipping processor and a frame buffer. The method includes: organizing
  and storing of NURBS data in system memory as a sequence of data records
  such that successive spans of a parametric curve of order k are defined
  by successive individual data records in conjunction with the immediately
  preceding 2k-3 prior data records; transforming the control points from
  modelling coordinates to view coordinates (x,y,z); multiplying the
  transformed control point coordinates by a weight yielding wx, wy, wz, w;
  simultaneously within each parallel floating point processor evaluating
  the b-spline functions for one component of the coordinate set (wx, wy,
  wz, w) for determined parameter points; eliminating the weight from wx,
  wy, wz, w yielding geometric coordinates x,y,z for points on the curve,
  clipping the geometric coordinates to the current viewing boundaries and
  drawing the clipped vectors as straight line segments on a screen of a
  computer graphics display system.   (see image in original document)
ABSTRACT WORD COUNT: 196

LEGAL STATUS (Type, Pub Date, Kind, Text):
  Application: 910502 A2 Published application (Alwith Search Report
                             ;A2without Search Report)
  Examination: 910502 A2 Date of filing of request for examination:
                             901213
  Change: 910918 A2 Representative (change)
  Search Report: 921007 A3 Separate publication of the European or
                             International search report
  Change: 921216 A2 Representative (change)
  Examination: 951206 A2 Date of despatch of first examination report:
                             951019
  Withdrawal: 971112 A2 Date on which the European patent application
                             was deemed to be withdrawn: 970522
LANGUAGE (Publication,Procedural,Application): English; English; English

27/5/14   (Item 14 from file: 348)
DIALOG(R)File 348:European Patents

00389650
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
Parallel processor structure for the implementation and learning of artificial neuronal networks.
Parallelrechnerstruktur zum Modellieren und Trainieren kunstlicher Neuronaler Netze.
Structure de processeurs parallele pour la realisation et l'apprentissage de reseaux neuronaux artificiels.
PATENT ASSIGNEE:
  Bodenseewerk Geratetechnik GmbH, (435830), Alte Nussdorfer Strasse 15
    Postfach 1120, D-7770 Uberlingen/Bodensee, (DE), (applicant designated
    states: BE;DE;FR;GB;NL)
INVENTOR:
  Hausing, Michael, Dr.-Ing., Strandweg 29 A, D-7770 Uberlingen, (DE)
  Hesse, HansKlaus, Dr.-Ing., Im Gehren 20, D-7770 Uberlingen, (DE)
LEGAL REPRESENTATIVE:
  Weisse, Jurgen, Dipl.-Phys. et al (12901), Bokenbusch 41 Postfach 11 03
    86, D-5620 Velbert 11-Langenberg, (DE)
PATENT (CC, No, Kind, Date): EP 388806 A2 900926 (Basic)
                              EP 388806 A3 920108
APPLICATION (CC, No, Date):   EP 90104969 900316;
PRIORITY (CC, No, Date): DE 3909153 890321
DESIGNATED STATES: BE; DE; FR; GB; NL
INTERNATIONAL PATENT CLASS: G06F-015/80;
CITED PATENTS (EP A): EP 377221 A
CITED REFERENCES (EP A):
  THE COMPUTER JOURNAL.   Bd. 30, Nr. 5, Oktober
    1987, LONDON GB Seiten 413 - 419; FORREST: 'Implementing neural network
    models on parallel computers'
  IEEE INTERNATIONAL CONFERENCE ON COMMUNICATIONS 87 Bd. 2, 7. Juni 1987,
    SEATTLE,USA Seiten 853 - 857; CIOFFI: 'A pipelined fast QR-RLS
    structure for high-speed VLSI implementation of adaptive filters'
  PROCEEDINGS OF THE 26TH IEEE CONFERENCE ON   DECISION AND CONTROL Bd.
    2, 9. Dezember 1987, LOS ANGELES, USA Seiten 1461 - 1467; KUNG:
    'Systolic designs for state space models : Kalman filtering and neural
    network';

ABSTRACT EP 388806 A2 (Translated)
  A parallel processor structure for modelling and training artificial
neuronal networks is connected to a host computer and constructed as
two-dimensional matrix of simple identical processor elements. The
processor elements are supplied with a command stream by a sequencer in
accordance with the SIMD principle. The processor elements arranged on
the diagonals of the matrix are allocated to the nodes of the neuronal
network and intended for carrying out the neuronal functions. The
non-diagonal processor elements handle the logic combinations between the
nodes and are selected for the function of the variable synaptic
weightings. The matrix firstly has a local neighbourhood networking to
the four next neighbouring processors in each case. In addition, lines
come from the neuronal processors, separated in x and y direction, which
drive the non-diagonal synapse processors in parallel. In one direction,
these lines are used for accelerating the distribution of the calculation
results of the neuronal processors to the synapse processors. In the
other direction, the lines are used for the accelerated distribution of
correction data during the learning process.
TRANSLATED ABSTRACT WORD COUNT: 177

ABSTRACT EP 388806 A2
    Eine Parallelrechnerstruktur zum Modellieren und Trainieren kunstlicher
  Neuronaler Netze ist an einen Host-Rechner angeschlossen und als

zweidimensionale Matrix aus einfachen, identischen Prozessorelementen ausgebildet. Die Prozessorelemente werden nach dem SIMD-Prinzip von einem Sequencer mit einem Befehlsstrom versorgt. Die auf der Diagonalen der Matrix angeordneten Prozessorelemente werden den Knoten des Neuronalen Netzes zugeordnet und zur Durchfuhrung der Neuronenfunktionen bestimmt. Die nichtdiagonalen Prozessorelemente ubernehmen die Verknupfungen zwischen den Knoten und werden fur die Funktion der veranderbaren synaptischen Gewichtungen bestimmt. Die Matrix besitzt erstens eine lokale Nachbarschaftsvernetzung zu den jeweils vier nachsten Nachbarprozessoren. Daruber hinaus gehen von den Neuronenprozessoren, getrennt nach x- und y-Richtung Leitungen aus, welche die nicht-diagonalen Synapsenprozessoren parallel ansteuern. In der einen Richtung dienen diese Leitungen der Beschleunigung der Verteilung der Berechnungsergebnisse der Neuronenprozessoren an die Synapsenprozessoren. In der anderen Richtung dienen die Leitungen der beschleunigten Verteilung der Korrekturdaten wahrend des Trainings.
ABSTRACT WORD COUNT: 145

LEGAL STATUS (Type, Pub Date, Kind, Text):
 Application: 900926 A2 Published application (A1with Search Report
                              ;A2without Search Report)
 Search Report: 920108 A3 Separate publication of the European or
                              International search report
 Examination: 920826 A2 Date of filing of request for examination:
                              920620
 Examination: 930421 A2 Date of despatch of first examination report:
                              930304
 Withdrawal: 940105 A2 Date on which the European patent application
                              was deemed to be withdrawn: 930715
LANGUAGE (Publication,Procedural,Application): German; German; German
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(German)	EPABF1	455
SPEC A	(German)	EPABF1	2594
Total word count - document A			3049
Total word count - document B			0
Total word count - documents A + B			3049

 27/5/15   (Item 15 from file: 348)
DIALOG(R)File 348:European Patents
(c) 2000 European Patent Office. All rts. reserv.

00362434
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
Remote boot
Fern-Urlader
Chargement initial a distance
PATENT ASSIGNEE:
  DIGITAL EQUIPMENT CORPORATION, (313081), 111 Powdermill Road, Maynard
    Massachusetts 01754-1418, (US), (applicant designated states:
    DE;FR;GB;NL)
INVENTOR:
  Flaherty, James E., 168 White Pond Road, Hudson Massachusetts 01749, (US)
LEGAL REPRESENTATIVE:
  Goodman, Christopher et al (31122), Eric Potter & Clarkson St. Mary's
    Court St. Mary's Gate, Nottingham NG1 1LE, (GB)
PATENT (CC, No, Kind, Date):   EP 358292   A2   900314 (Basic)
                               EP 358292   A3   900829
                               EP 358292   B1   970910
APPLICATION (CC, No, Date):   EP 89302132 890303;
PRIORITY (CC, No, Date): US 240955 880906

DESIGNATED STATES: DE; FR; GB; NL
INTERNATIONAL PATENT CLASS: G06F-009/445; G06F-015/16; G06F-009/44;

ABSTRACT EP 358292 A2
    A system and method of down loading, over a network, operating systems
or other executable programs to a computer which does not have a boot
device or other device containing the executable program. Down loading is
accomplished without modification of the loadable image. The computer has
a network interface which requests a minimum-boot program be transferred
from a host computer on the network. The minimum-boot program, when
executed, establishes a logical connection to a disk server on the
network and allows the requesting computer to treat the disk server as a
local boot device.
ABSTRACT WORD COUNT: 98

LEGAL STATUS (Type, Pub Date, Kind, Text):
 Application: 900314 A2 Published application (A1with Search Report
                               ;A2without Search Report)
 Examination: 900314 A2 Date of filing of request for examination:
                               890316
 Search Report: 900829 A3 Separate publication of the European or
                               International search report
 Examination: 941214 A2 Date of despatch of first examination report:
                               941028
 Grant: 970910 B1 Granted patent
 Oppn None: 980902 B1 No opposition filed
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language   Update   Word Count
      CLAIMS B (English)   9709W1   1415
      CLAIMS B (German)   9709W1   1264
      CLAIMS B (French)   9709W1   1708
      SPEC B   (English)   9709W1   3551
Total word count - document A   0
Total word count - document B   7938
Total word count - documents A + B   7938

 27/5/16   (Item 16 from file: 348)
DIALOG(R)File 348:European Patents
(c) 2000 European Patent Office. All rts. reserv.

00333245
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
**HIGH PERFORMANCE GRAPHICS WORKSTATION AND METHOD OF OPERATING THEREFOR
HOCHLEISTUNGSFAHIGES GRAPHISCHES ENDGERAT SOWIE BETRIEBSVERFAHREN DAFUR
POSTE DE TRAVAIL GRAPHIQUE A HAUTE PERFORMANCE ET METHODE D'EXPLOITATION
   POUR CELA**
PATENT ASSIGNEE:
  DIGITAL EQUIPMENT CORPORATION, (313081), 111 Powdermill Road, Maynard
    Massachusetts 01754-1418, (US), (applicant designated states:
    DE;FR;GB;IT;NL)
INVENTOR:
  DOYLE, Peter, Lawrence, 279 Davis Street, Northboro, MA 01532, (US)
  ELLENBERGER, John, Philipp, 296 Nashua Road, Groton, MA 01450, (US)
  JONES, Ellis, Olivier, 124 Rattlesnake Hill Road, Andover, MA 01810, (US)
  CARVER, David, C., 6 Independence Avenue, Lexington, MA 02173, (US)
  DIPIRRO, Steven, D., 270 High Street, Holliston, MA 01746, (US)
  GEROVAC, Branko, J., 116 Boston Post Road, Marlboro, MA 01752, (US)
  ARMSTRONG, William, Paul, 7080 South 2870 East, Salt Lake City, UT 84121,
    (US)
  GIBSON, Ellen, Sarah, 839 East South Temple, Salt Lake City, UT 84102,

(US)
SHAPIRO, Raymond, Elliott, 29 Hunter Avenue, Marlboro, MA 01752, (US)
RUSHFORTH, Kevin, C., 450 N Mathilda Ave S207, Sunnyvale, CA 94086, (US)
ROACH, William, C., 580 Arapeen Drive, Salt Lake City, UT 84108, (US)
LEGAL REPRESENTATIVE:
  Betten, Jurgen, Dipl.-Ing. et al (38515), Betten & Resch Patentanwalte
    Reichenbachstrasse 19, D-80469 Munchen, (DE)
PATENT (CC, No, Kind, Date):   EP 329771 A1   890830 (Basic)
                               EP 329771 B1   960424
                               WO 8901664   890223
APPLICATION (CC, No, Date):   EP 88908489 880812; WO 88US2727 880812
PRIORITY (CC, No, Date): US 85081 870813
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: G06T-017/00;
CITED PATENTS (WO A): US 4315310 A; US 4509115 A
CITED REFERENCES (EP A):
  See also references of WO8901664;

ABSTRACT EP 329771 A1
    A high performance graphics workstation includes a digital computer
  host and a graphics subsystem. Two- and three-dimensional graphics data
  structures, built by the host, are stored in the graphics subsystem. The
  asynchronous traversal of the data structures together with traversal
  control functions coordinate and control the flow of graphics data and
  commands to a graphics pipeline for processing and display. The address
  space of the graphics subsystem is mapped into a reversed I/O space of
  the host. This permits the host to directly access the graphics
  subsystem.
ABSTRACT WORD COUNT: 91
NOTE:
  No A-document published by EPO

LEGAL STATUS (Type, Pub Date, Kind, Text):
  Application: 890830 A1 Published application (A1with Search Report
                              ;A2without Search Report)
  Examination: 890830 A1 Date of filing of request for examination:
                              890502
  Change: 891025 A1 Inventor (change)
  Change: 900307 A1 Inventor (change)
  Examination: 920311 A1 Date of despatch of first examination report:
                              920123
  Grant: 960424 B1 Granted patent
  Oppn None: 970416 B1 No opposition filed
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language   Update   Word Count
      CLAIMS A (English)   EPABF1   2343
      CLAIMS B (English)   EPAB96   1122
      CLAIMS B   (German)   EPAB96   988
      CLAIMS B   (French)   EPAB96   1290
      SPEC A   (English)   EPABF1   18501
      SPEC B   (English)   EPAB96   18699
Total word count - document A   20846
Total word count - document B   22099
Total word count - documents A + B   42945

 27/5/17   (Item 17 from file: 348)
DIALOG(R)File 348:European Patents
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00317499

                      25 May 10, 2000 10:32

ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
Computer graphic apparatus for processing lighting model information.
Rechnergraphikgerat zur Verarbeitung von Beleuchtungsmodellinformation.
Appareil graphique a calculateur pour le traitement d'information de modele
  d'eclairage.
PATENT ASSIGNEE:
  International Business Machines Corporation, (200120), Old Orchard Road,
    Armonk, N.Y. 10504, (US), (applicant designated states: DE;FR;GB;IT)
INVENTOR:
  Gonzalez-Lopez, Jorge, 8 Hewlett Road, Red Hook New York 12571, (US)
  Hempel, Bruce Carlton, Lasher Road, Tivoli New York 12583, (US)
  Liang, Bob Chao-Chu, Ryan Drive, West Hurley New York 12491, (US)
LEGAL REPRESENTATIVE:
  Burt, Roger James, Dr. et al (52152), IBM United Kingdom Limited
    Intellectual Property Department Hursley Park, Winchester Hampshire
    SO21 2JN, (GB)
PATENT (CC, No, Kind, Date): EP 314341 A2 890503 (Basic)
                              EP 314341 A3 910724
                              EP 314341 B1 950315
APPLICATION (CC, No, Date):   EP 88309573 881013;
PRIORITY (CC, No, Date): US 115467 871030
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: G06T-011/00;
CITED PATENTS (EP A): US 4343037 A; EP 193151 A

ABSTRACT EP 314341 A2
    A lighting model processing system for a computer graphics
  workstation's shading function includes multiple floating point
  processing stages arranged and operated in pipeline. Each stage is
  constructed from one or more identical floating point processors. The
  lighting model processing system supports one or more light sources
  illuminating an object to be displayed, with parallel or perspective
  projection. Dynamic partitioning can be used to balance the computational
  workload among various of the processors in order to avoid a bottleneck
  in the pipeline. The high throughput of the pipeline system makes
  possible the rapid calculation and display of high quality shaded images.

ABSTRACT WORD COUNT: 104

LEGAL STATUS (Type, Pub Date, Kind, Text):
 Application: 890503 A2 Published application (A1with Search Report
                             ;A2without Search Report)
 Examination: 891004 A2 Date of filing of request for examination:
                             890809
 Change: 891025 A2 Representative (change)
 Search Report: 910724 A3 Separate publication of the European or
                             International search report
 Change: 910814 A2 Representative (change)
 Change: 930324 A2 Representative (change)
 Examination: 931020 A2 Date of despatch of first examination report:
                             930907
 Grant: 950315 B1 Granted patent
 Oppn None: 960306 B1 No opposition filed
 Lapse: 991020 B1 Date of lapse of European Patent in a
                             contracting state (Country, date):   IT
                             19950315,
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language   Update   Word Count
       CLAIMS A (English) EPABF1   832
       CLAIMS B (English) EPAB95   515
       CLAIMS B (German)   EPAB95   478

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        CLAIMS B    (French)   EPAB95      603
        SPEC A      (English)  EPABF1     5584
        SPEC B      (English)  EPAB95     8694
Total word count - document A          6416
Total word count - document B         10290
Total word count - documents A + B    16706
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27/5/18   (Item 18 from file: 348)
DIALOG(R)File 348:European Patents
(c) 2000 European Patent Office. All rts. reserv.

00298774
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
Single node image for a multiple processor network node.
Vorstellung des Bildes eines einzigen Knotens fur einen Netzwerkknoten mit
   mehreren Prozessoren.
Presentation de l'image d'un noeud unique pour un noeud de reseau avec
   plusieurs processeurs.
PATENT ASSIGNEE:
   International Business Machines Corporation, (200120), Old Orchard Road,
      Armonk, N.Y. 10504, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
   Halim, Nagui, 1845 Maple Hill Street, Yorktown Heights, N.Y. 10598, (US)
   Nikolaou, Christos Nicholas, 121 West 79th Street, Apt. 1R, New York,
      N.Y. 10024, (US)
   Pershing Jr., John Arthur, 29-C Scenic Drive, Croton-on-Hudson, N.Y.
      10521, (US)
LEGAL REPRESENTATIVE:
   Jost, Ottokarl, Dipl.-Ing. (6092), IBM Deutschland Informationssysteme
      GmbH, Patentwesen und Urheberrecht, D-70548 Stuttgart, (DE)
PATENT (CC, No, Kind, Date):   EP 314909   A2   890510 (Basic)
                               EP 314909   A3   911030
                               EP 314909   B1   950308
APPLICATION (CC, No, Date):   EP 88115361 880920;
PRIORITY (CC, No, Date): US 116424 871103
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G06F-015/16;
CITED PATENTS (EP A): EP 118037 A
CITED REFERENCES (EP A):
   DATA COMMUNICATIONS. vol. 16, no. 2, February 1987, NEW YORK US pages 116
      - 134; T.J.Routt: "A network architecture gets on track"
   Proceedings IEEE/AIAA 7th didital avionics systems conference 13 October
      1986, Fort Worth, Texas, US pages 536 - 544; D.B.Evans: "Fault tolerant
      high-speed switched data network"
   IBM TECHNICAL DISCLOSURE BULLETIN. vol. 28, no. 8, January 1986, NEW YORK
      US pages 3513 - 3517; "Establishing virtual circuits in large computer
      networks";

ABSTRACT EP 314909 A2
   A method and apparatus for coupled computer systems provides a single
network node image when connected to a computer network, so that the
network is unaware of the "fine" structure of the computer systems in the
machine room. The coupled complex is made available to the network.
ABSTRACT WORD COUNT: 51

LEGAL STATUS (Type, Pub Date, Kind, Text):
 Application: 890510 A2 Published application (A1with Search Report
                             ;A2without Search Report)
 Examination: 891102 A2 Date of filing of request for examination:
                             890906
 Search Report: 911030 A3 Separate publication of the European or

International search report
Change: 930512 A2 Representative (change)
Examination: 931222 A2 Date of despatch of first examination report:
                          931104
Grant: 950308 B1 Granted patent
Oppn None: 960228 B1 No opposition filed
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language   Update   Word Count
     CLAIMS A   (English)   EPABF1   300
     CLAIMS B   (English)   EPAB95   337
     CLAIMS B   (German)   EPAB95   331
     CLAIMS B   (French)   EPAB95   418
     SPEC A   (English)   EPABF1   9800
     SPEC B   (English)   EPAB95   9738
Total word count - document A   10101
Total word count - document B   10824
Total word count - documents A + B   20925

 27/5/19   (Item 19 from file: 348)
DIALOG(R)File 348:European Patents
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00298509
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
**An aperiodic mapping method to enhance power-of-two stride access to
   interleaved devices.**
**Nichtperiodisches Abbildungsverfahren zum verbesserten Zweierpotenzzugriff
   fur ineinandergreifende Einrichtungen.**
**Methode de transformation aperiodique pour ameliorer l'acces, par pas de
   puissance de deux, a des dispositifs entrelaces.**
PATENT ASSIGNEE:
  International Business Machines Corporation, (200120), Old Orchard Road,
     Armonk, N.Y. 10504, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
  McAuliffe, Kevin Patrik, 3517 Strang Boulevard, Yorktown Heights N.Y.
     10598, (US)
  Melton, Evelyn Au, 20 Rothenburg Road, Poughkeepsie New York 12603, (US)
  Norton, Vern Alan, 11 Ridge Road, Croton-on-Hudson New York 10520, (US)
  Pfister, Gregory Francis, 780 Pleasantville Road, Briarcliff Manor New
     York 10510, (US)
  Wakefield, Scott Philip, 44 Hunter Place, Croton-on-Hudson New York 12520
     , (US)
LEGAL REPRESENTATIVE:
  Schafer, Wolfgang, Dipl.-Ing. (62021), IBM Deutschland
     Informationssysteme GmbH Patentwesen und Urheberrecht, D-70548
     Stuttgart, (DE)
PATENT (CC, No, Kind, Date): EP 313788 A2 890503 (Basic)
                              EP 313788 A3 900801
                              EP 313788 B1 950621
APPLICATION (CC, No, Date):   EP 88115088 880915;
PRIORITY (CC, No, Date): US 114909 871029
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G06F-012/02;
CITED PATENTS (EP A): EP 179401 A; US 4400768 A
CITED REFERENCES (EP A):
  TRANSACTIONS OF THE I.E.C.E. OF JAPAN, vol. E65, no. 8, August 1982,
     pages 464-471; S. SHIMIZU et al.: "A new addressing scheme with
     reorganizable memory structure -basic principle-"
  THE 13TH ANNUAL INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE, Tokyo,
     2nd - 5th June 1986, pages 324-328, IEEE, New York, US; D.T. HARPER et

al.: "Performance evaluation of vector accesses in parallel memories using a skewed storage scheme"
IBM TECHNICAL DISCLOSURE BULLETIN, vol. 25, no. 8, January 1983, pages 4445-4449, New York, US; R.N. LANGMAID: "Versatile programmable logic array";

ABSTRACT EP 313788 A2
An aperiodic mapping procedure for the mapping of logical to physical addresses is defined as a permutation function for generating optimized stride accesses in an interleaved multiple device system such as a large, parallel processing shared memory system wherein the function comprises a bit-matrix multiplication of a presented first (logical) address with a predetermined matrix to produce a second (physical) address. The permutation function maps the address from a first to a second address space for improved memory performance in such an interleaved memory system. Assuming that the memory has n logical address bits and $2(\sup(d)$ separately accessible memory devices (where $d <= n$) and a second address that utilizes $n - d$ bits of the first address as the offset within the referenced device node. The procedure includes performing a bit matrix multiplication between successive rows of the said matrix and bits of the first address to produce successive d bits of the second address.
ABSTRACT WORD COUNT: 161

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application:	890503	A2	Published application (A1with Search Report ;A2without Search Report)
Examination:	891004	A2	Date of filing of request for examination: 890809
Search Report:	900801	A3	Separate publication of the European or International search report
Examination:	921223	A2	Date of despatch of first examination report: 921109
Grant:	950621	B1	Granted patent
Lapse:	960501	B1	Date of lapse of the European patent in a Contracting State: FR 951117
Oppn None:	960612	B1	No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	560
CLAIMS B	(English)	EPAB95	551
CLAIMS B	(German)	EPAB95	493
CLAIMS B	(French)	EPAB95	645
SPEC A	(English)	EPABF1	7639
SPEC B	(English)	EPAB95	7662
Total word count - document A			8199
Total word count - document B			9351
Total word count - documents A + B			17550

27/5/20   (Item 20 from file: 348)
DIALOG(R)File 348:European Patents
(c) 2000 European Patent Office. All rts. reserv.

00284770
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
Raster display vector generator.
Vektorgenerator fur Raster-Bildschirmanzeige.
Generateur de trace de vecteur pour l'affichage video a balayage par trame.
PATENT ASSIGNEE:
International Business Machines Corporation, (200120), Old Orchard Road, Armonk, N.Y. 10504, (US), (applicant designated states: DE;FR;GB;IT)

29 May 10, 2000 10:32

INVENTOR:
  Lumelsky, Leon, 30 Gaxton Road, Stamford Connecticut 06905, (US)
LEGAL REPRESENTATIVE:
  Burt, Roger James, Dr. (52152), IBM United Kingdom Limited Intellectual
    Property Department Hursley Park, Winchester Hampshire SO21 2JN, (GB)
PATENT (CC, No, Kind, Date):   EP 279227 A2 880824 (Basic)
                               EP 279227 A3 910417
                               EP 279227 B1 940518
APPLICATION (CC, No, Date):   EP 88101080 880126;
PRIORITY (CC, No, Date): US 13848 870212
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: G09G-001/16; G09G-005/36;
CITED PATENTS (EP A): US 4642625 A; EP 164880 A; US 4580236 A; WO 8500679 A
  ; US 3906480 A

ABSTRACT EP 279227 A2
    A vector generator for use with an all-points-addressable frame buffer
  capable of the non-word aligned access, simultaneously, of a square M by
  N array of pixels providing fast vector drawing independently of vector
  slope and position in the whole screen area of an attached display
  monitor. The vector generator utilises a triangular logic matrix together
  with a line drawing unit to generate M vector bits lying in an M by N
  square matrix of the screen of an attached monitor in one memory cycle of
  the frame buffer and uses the generated matrix to generate a direct mask
  for the frame buffer whereby the M bit vector may be stored in a single
  memory cycle.
ABSTRACT WORD COUNT: 119

LEGAL STATUS (Type, Pub Date, Kind, Text):
  Application: 880824 A2 Published application (A1with Search Report
                             ;A2without Search Report)
  Examination: 890125 A2 Date of filing of request for examination:
                             881130
  Change: 910410 A2 Obligatory supplementary classification
                             (change)
  Search Report: 910417 A3 Separate publication of the European or
                             International search report
  Change: 910710 A2 Representative (change)
  Examination: 921104 A2 Date of despatch of first examination report:
                             920922
  Change: 930331 A2 Representative (change)
  Grant: 940518 B1 Granted patent
  Oppn None: 950510 B1 No opposition filed
  Lapse: 970423 B1 Date of lapse of the European patent in a
                             Contracting State: FR 960930, GB 960126
  Lapse: 991020 B1 Date of lapse of European Patent in a
                             contracting state (Country, date):   IT
                             19940518,
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language   Update   Word Count
      CLAIMS B (English)   EPBBF1   666
      CLAIMS B (German)   EPBBF1   610
      CLAIMS B (French)   EPBBF1   806
      SPEC B   (English)   EPBBF1   6847
Total word count - document A   0
Total word count - document B   8929
Total word count - documents A + B   8929

27/5/21   (Item 21 from file: 348)
DIALOG(R)File 348:European Patents

30 May 10, 2000 10:32

00282118
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
DATAFLOW PROCESSING ELEMENT, MULTIPROCESSOR, AND PROCESSES.
DATENFLUSSVERARBEITUNGSELEMENT-MULTIPROZESSOR UND -VERFAHREN.
ELEMENT DE TRAITEMENT DE FLUX DE DONNEES, MULTIPROCESSEUR ET PROCEDES.
PATENT ASSIGNEE:
  DENNIS, Jack B., (948130), 55 Wellesley Road, Belmont, MA 02178, (US),
    (applicant designated states: BE;CH;DE;FR;GB;IT;LI;NL;SE)
INVENTOR:
  DENNIS, Jack B., 55 Wellesley Road, Belmont, MA 02178, (US)
LEGAL REPRESENTATIVE:
  Driver, Virginia Rozanne et al (58901), Haseltine Lake & Co. Hazlitt
    House 28 Southampton Buildings Chancery   Lane, London WC2A 1AT, (GB)
PATENT (CC, No, Kind, Date): EP 315647 A1 890517 (Basic)
                              EP 315647 A1 910130
                              WO 8800732 880128
APPLICATION (CC, No, Date):   EP 87905809 870713; WO 87US1668 870713
PRIORITY (CC, No, Date): US 885836 860715
DESIGNATED STATES: BE; CH; DE; FR; GB; IT; LI; NL; SE
INTERNATIONAL PATENT CLASS: G06F-003/00; G06F-009/30; G06F-009/36;
  G06F-009/38; G06F-009/40; G06F-013/00;
CITED PATENTS (WO A): US 4153932 A; US 4197589 A; US 4644461 A; US 4591979
  A; US 4413318 A
CITED REFERENCES (EP A):
  PROCEEDINGS 3RD CONFERENCE ON DIGITAL AVIONICS SYSTEMS, Fortworth, Texas,
    November 1979, pages 19-25, IEEE, New York, US; M. CORNISH et al.: "The
    TI data flow architectures: The power of concurrency for avionics"
  THE COMPUTER JOURNAL, vol. 25, no. 2, May 1982, pages 207-217; P.C.
    TRELEAVEN et al.: "Combining data flow and control flow computing"
  See also references of WO8800732;
CITED REFERENCES (WO A):
  JENKINS, RICHARD A., "Supercomputers of Today and Tommorrow", Tab Books
    Inc., BLue Ridge Summit, PA., 1986, pp. 92-94.
  REISIG, WOLFGANG, "Petri Nets", New York, NY, 1982, Chapters 1 and 3.
  HWANG, KAI and BRIGGS, FAYE A., "Computer Architecture and Parallel
    Processing",Mcgraw Hill, Inc., NY, 1984, Sections 10.1 and 10.2.;
NOTE:
  No A-document published by EPO
LEGAL STATUS (Type, Pub Date, Kind, Text):
 Application: 890517 A1 Published application (A1with Search Report
                           ;A2without Search Report)
 Examination: 890517 A1 Date of filing of request for examination:
                           890113
 Change: 890830 A1 Representative (change)
 Search Report: 910130 A1 Drawing up of a supplementary European search
                           report: 901211
 Withdrawal: 930804 A1 Date on which the European patent application
                           was deemed to be withdrawn: 930202
LANGUAGE (Publication,Procedural,Application): English; English; English

 27/5/22   (Item 22 from file: 348)
DIALOG(R)File 348:European Patents

00238836
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
Computer.
Rechner.
Ordinateur.

PATENT ASSIGNEE:
  Thomas, Gerhard G., (843610), Weinmeisterhornweg 80, D-1000 Berlin 20,
    (DE), (applicant designated states: CH;DE;FR;GB;IT;LI;SE)
  Mitterauer, Bernhard Dr., (843620), Viehhausen 59, A-5071 Wals bei
    Salzburg, (AT), (applicant designated states: CH;DE;FR;GB;IT;LI;SE)
INVENTOR:
  Thomas, Gerhard G., Weinmeisterhornweg 80, D-1000 Berlin 20, (DE)
  Mitterauer, Bernhard Dr., Viehhausen 59, A-5071 Wals bei Salzburg, (AT)
LEGAL REPRESENTATIVE:
  Haft, Berngruber, Czybulka , Postfach 14 02 46, D-8000 Munchen 5, (DE)
PATENT (CC, No, Kind, Date): EP 235764 A2 870909 (Basic)
                              EP 235764 A3 880907
APPLICATION (CC, No, Date):   EP 87102829 870227;
PRIORITY (CC, No, Date): DE 3607241 860305
DESIGNATED STATES: CH; DE; FR; GB; IT; LI; SE
INTERNATIONAL PATENT CLASS: G06F-015/06
CITED PATENTS (EP A): DE 3429078 A; US 4518866 A; EP 132926 A; US 3473160 A
CITED REFERENCES (EP A):
  SUPPLEMENTO AI RENDICONTI DEL CIRCOLO MATEMATICO DI PALERMO, Serie II/2,
    1982, Seiten 275-286; G.G. THOMAS: "On permutographs"
  PROCEEDINGS OF THE ASSOCIATION FOR COMPUTING MACHINERY, San Francisco,
    CA, 8.-14. Oktober 1984, Seiten 212-221, North-Holland/ACM, Amsterdam,
    NL; D.I. MOLDOVAN: "An associative array architecture intended for
    semantic network processing";

ABSTRACT EP 235764 A2
    Rechner.
    Die Erfindung bezieht sich auf einen Rechner, insbesondere zur
  Simulation biologischer Prozesse. Kernstuck des Rechners ist ein
  zentrales Logik/Rechensystem (2), das als n-wertiger Permutograph
  aufgebaut ist. Das Negationsnetz dieses Permutographen besteht aus
  einzelnen Knotenrechnern, die uber Informations- bzw. Negationsleitungen
  (22, 32) mit anderen Knotenrechnern verbunden sind. In jedem
  Knotenrechner (21) ist das Negationsnetz des Permutographen in einer
  Subknoteneinheit (26) enthalten. Der Gesamtrechner kann von aussen oder
  intern gesteuert werden, so dass sich ein intentionaler Rechner ergibt.
ABSTRACT WORD COUNT: 79
LEGAL STATUS (Type, Pub Date, Kind, Text):
  Application: 870909 A2 Published application (A1with Search Report
                             ;A2without Search Report)
  Change: 880817 A2 International patent classification (change)
  Search Report: 880907 A3 Separate publication of the European or
                             International search report
  Examination: 890315 A2 Date of filing of request for examination:
                             890116
  Examination: 901031 A2 Date of despatch of first examination report:
                             900918
  Withdrawal: 930714 A2 Date on which the European patent application
                             was deemed to be withdrawn: 930120
LANGUAGE (Publication,Procedural,Application): German; German; German

  27/5/23   (Item 23 from file: 348)
DIALOG(R)File 348:European Patents
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00217101
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
Switching system for transmission of data.
Vermittlungssystem fur Datenubertragung.
Systeme de commutation pour la transmission de donnees.
PATENT ASSIGNEE:

International Business Machines Corporation, (200120), Old Orchard Road, Armonk, N.Y. 10504, (US), (applicant designated states: DE;FR;GB;IT)
INVENTOR:
  Franaszek, Peter Anthony, P.O. Box 218, Yorktown Heights, New York 10598, (US)
LEGAL REPRESENTATIVE:
  Atchley, Martin John Waldegrave (27831), IBM United Kingdom Limited Intellectual Property Department Hursley Park, Winchester Hampshire SO21 2JN, (GB)
PATENT (CC, No, Kind, Date): EP 195589 A2 860924 (Basic)
                              EP 195589 A3 890719
                              EP 195589 B1 920610
APPLICATION (CC, No, Date):   EP 86301778 860312;
PRIORITY (CC, No, Date): US 713117 850318
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: G06F-015/16; H04Q-003/68;
CITED REFERENCES (EP A):
  AFIPS CONFERENCE PROCEEDINGS, Chicago, Illinois, 4th-7th May 1981, pages 125-135, AFIPS Press, Arlington, Virginia, US; B. QUATEMBER: "Modular crossbar switch for large-scale multiprocessor systems-structure and implementation"
  MICROPROCESSORS AND MICROSYSTEMS, vol. 7, no. 2, March 1983, pages 75-79, Butterworth & Co., (Publishers) Ltd, Whitstable, Kent, GB; B. WILKINSON et al.: "Cross-bar switch multiple microprocessor system"
  COMPUTER, vol. 14, no. 12, December 1981, pages 43-53, IEEE, Long Beach, CA, US; D.M. DIAS et al.: "Packet switching interconnection networks for modular systems"
  IBM TECHNICAL DISCLOSURE BULLETIN, vol. 25, no. 7A, December 1982, pages 3578-3582, New York, US; E.R. MARSH: "Data base control and processing system";

ABSTRACT EP 195589 A2
  A switching system for transmission of data comprises a switching matrix (34) partitioned into a plurality of selectable data transmission paths, these paths providing connections between each of a plurality of first ports of the matrix and selected ones of a plurality of second ports of the matrix, first path control means (30, 40) for controlling each data transmission path for completing each selected connection, and system control means (32, 42) responsive to a message requesting a connection between a first port and a selected second port to establish the requested connection,
  The switching system is characterised in that the system control means provides for the establishment of the requested connection beginning at a determined time based upon prior established connections to the selected second port, and the path control means (40) establishes the requested connection at the determined time so as to provide for transmission of data from the first port to the selected second port.
ABSTRACT WORD COUNT: 161

LEGAL STATUS (Type, Pub Date, Kind, Text):
  Application: 860924 A2 Published application (A1with Search Report ;A2without Search Report)
  Examination: 870325 A2 Date of filing of request for examination: 870116
  Search Report: 890719 A3 Separate publication of the European or International search report
  Examination: 910710 A2 Date of despatch of first examination report: 910527
  Grant: 920610 B1 Granted patent
  Oppn None: 930602 B1 No opposition filed
  Lapse: 970423 B1 Date of lapse of the European patent in a Contracting State: DE 961203

Lapse: 991020 B1 Date of lapse of European Patent in a
                                  contracting state (Country, date):   IT
                                  19920610,
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language   Update   Word Count
     CLAIMS B (English)   EPBBF1   738
     CLAIMS B (German)   EPBBF1   645
     CLAIMS B (French)   EPBBF1   921
     SPEC B   (English)   EPBBF1   12881`
Total word count - document A   0
Total word count - document B   15185
Total word count - documents A + B   15185

 27/5/24   (Item 24 from file: 348)
DIALOG(R)File 348:European Patents
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00160956
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
Computer systems for curve-solid classification and solid modeling.
Rechnersysteme zur Kurvenkorperklassifizierung und Korpermodellierung.
Systemes de calculateurs pour la classification de solides courbes et la
   modelisation de solides.
PATENT ASSIGNEE:
  THE UNIVERSITY OF ROCHESTER, (290263), Office of Research and Project
     Administration, 30 Administration Building, Rochester, New York 14627,
     (US), (applicant designated states: AT;BE;CH;DE;FR;GB;IT;LI;LU;NL;SE)
INVENTOR:
  Kedem, Gershon, 275 Ashbourne Road, Rochester, N.Y. 14618, (US)
  Ellis, John L., 226 Jeffords Road, Rush, N.Y. 14543, (US)
LEGAL REPRESENTATIVE:
  Wagner, Karl H. et al (12561), WAGNER & GEYER Patentanwalte
     Gewurzmuhlstrasse 5, D-80538 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 160848 A2 851113 (Basic)
                              EP 160848 A3 881005
                              EP 160848 B1 931201
APPLICATION (CC, No, Date):   EP 85104163 850404;
PRIORITY (CC, No, Date): US 608295 840508
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IT; LI; LU; NL; SE
INTERNATIONAL PATENT CLASS: G06F-015/72;
CITED REFERENCES (EP A):
  COMPUTER GRAPHICS AND IMAGE PROCESSING, vol. 18, no. 2, February 1982,
     pages 109-144, Academic Press Inc., New York, US; S.D. ROTH: "Ray
     casting for modeling solids"
  IBM TECHNICAL DISCLOSURE BULLETIN, vol. 23, no. 9, February 1981, pages
     3996-4005, New York, US; S. BOINODIRIS: "Computer graphics using
     multi-echelon processing structures";

ABSTRACT EP 160848 A2
   Computer systems for curve-solid classification and solid modeling.
   A computer system is introduced for curve-solid classification
(raycasting) of objects in constructive solid geometry (CSG) modeling to
produce image representations of two-and three-dimensional objects. The
system carries out curve-solid classifications in parallel and at much
higher speed than a general purpose computer. It uses primitive
classification processors which compute all of the (curveline or ray)
primitive (basic solid bodies: block, cylinder, etc.) intersections in
parallel, combine processors which are connected into a binary tree that
duplicates the binary tree defining the CSG solid and computes the set
operations (union, intersection and difference), and a host computer.

34 May 10, 2000 10:32

ABSTRACT WORD COUNT: 107

LEGAL STATUS (Type, Pub Date, Kind, Text):
 Lapse: 20000202 B1 Date of lapse of European Patent in a
                             contracting state (Country, date): AT
                             19931201, BE 19931201, CH 19931201, LI
                             19931201, IT 19931201, LU 19940430, NL
                             19931201, SE 19931201,
 Application: 851113 A2 Published application (A1with Search Report
                             ;A2without Search Report)
 Search Report: 881005 A3 Separate publication of the European or
                             International search report
 Examination: 890531 A2 Date of filing of request for examination:
                             890331
 *Assignee: 910313 A2 Applicant (transfer of rights) (change): THE
                             UNIVERSITY OF ROCHESTER (290263) Office of
                             Research and Project Administration, 30
                             Administration Building Rochester, New York
                             14627 (US) (applicant designated states:
                             AT;BE;CH;DE;FR;GB;IT;LI;LU;NL;SE)
 Examination: 910605 A2 Date of despatch of first examination report:
                             910424
 Grant: 931201 B1 Granted patent
 Lapse: 940803 B1 Date of lapse of the European patent in a
                             Contracting State: CH 931201, LI 931201
 Lapse: 940803 B1 Date of lapse of the European patent in a
                             Contracting State: CH 931201, LI 931201
 Lapse: 940928 B1 Date of lapse of the European patent in a
                             Contracting State: CH 931201, LI 931201, NL
                             931201
 Lapse: 941026 B1 Date of lapse of the European patent in a
                             Contracting State: CH 931201, LI 931201, NL
                             931201, SE 931201
 Lapse: 941117 B1 Date of lapse of the European patent in a
                             Contracting State: AT 931201, CH 931201, LI
                             931201, NL 931201, SE 931201
 Oppn None: 941123 B1 No opposition filed
 Lapse: 941130 B1 Date of lapse of the European patent in a
                             Contracting State: AT 931201, BE 931201, CH
                             931201, LI 931201, NL 931201, SE 931201
 Lapse: 970423 B1 Date of lapse of the European patent in a
                             Contracting State: AT 931201, BE 931201, CH
                             931201, LI 931201, GB 960404, NL 931201, SE
                             931201
 Lapse: 991020 B1 Date of lapse of European Patent in a
                             contracting state (Country, date): AT
                             19931201, BE 19931201, CH 19931201, LI
                             19931201, IT 19931201, NL 19931201, SE
                             19931201,
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language   Update   Word Count
     CLAIMS B   (English)   EPBBF1   880
     CLAIMS B   (German)   EPBBF1   844
     CLAIMS B   (French)   EPBBF1   1010
     SPEC B   (English)   EPBBF1   12470
Total word count - document A   0
Total word count - document B   15204
Total word count - documents A + B   15204

 27/5/25   (Item 25 from file: 348)

DIALOG(R)File 348:European Patents
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00145956
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
System and method for a data processing pipeline.
System und Verfahren zur Datenverarbeitungspipeline.
Systeme et methode pour un pipeline de traitement de donnees.
PATENT ASSIGNEE:
   Robert Bosch Corporation, P.O. Box 31816 2300 South 2300 West, Salt Lake
      City Utah 84131, (US), (applicant designated states: DE;FR;GB;IT)
INVENTOR:
   Andrews, David Heber, 6435 South Tresa Drive, West Jordan Utah 84084,
      (US)
   Lucht, Phillip H., 457 10th Avenue, Salt Lake City Utah 84103, (US)
   Putnam, Leland K., 4584 Driftwood Drive, Taylorsville Utah, (US)
LEGAL REPRESENTATIVE:
   Gibson, Stewart Harry et al (30972), URQUHART-DYKES & LORD Business
      Technology Centre Senghennydd Road, Cardiff CF2 4AY South Wales, (GB)
PATENT (CC, No, Kind, Date):   EP 146250   A2   850626 (Basic)
                               EP 146250   A3   871119
APPLICATION (CC, No, Date):   EP 84307611 841105;
PRIORITY (CC, No, Date): US 548312 831103
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: G06F-015/347; G06F-009/28;
CITED PATENTS (EP A): US 3816726 A; US 4208810 A; US 3763365 A
CITED REFERENCES (EP A):
   ELECTRONICS INTERNATIONAL, vol. 56, no. 21, October 1983, pages 113-119,
      New York, US; J.H. CLARK et al.: "Work station unites real-time
      graphics with unix, ethernet"
   S.M.P.T.E. JOURNAL, vol. 92, no. 9, September 1983, pages 912-917,
      Scarsdale, New York, US; J.A. BRIGGS: "Electronic graphics in
      television"
   IEEE TRANSACTIONS ON COMPUTERS, vol. C-25, no. 7, July 1976, pages
      703-712; J.J. CAPOWSKI: "The matrix transform processor";

ABSTRACT EP 146250 A2
      System and method for a data processing pipeline.
      A data processing system for processing encoded control points
   representing graphical illustrations, comprises a number of separate
   micro-programmed circuit cards, each of which are programmed to perform a
   specific processing operation.
      A command is first sent to a matrix maker card (201) defining a
   geometrical transformation to be performed on the graphical illustration.
   This card, thogehter with a matrix multiplier card (202), then calculates
   a transformation matrix representing the desired transformation.
      Electronic representations of control data points are then transmitted
   to the pipeline for processing and multiplied by the transformation
   matrix, computed previously, in a vector mulitplier circuit card (203).
   Next, the control points are clipped to the planes of a viewing frustum
   by a number of clipper cards (205-209), one card for each clipping plane.
   The 3D control points are then mapped onto the 2D viewing window by a
   viewpoint card (210).
      The clipped control points are then exploded to generate a plurality of
   small line segments representing each of the curved edges of the
   illustration. Finally, the appropriate portions of the illustration are
   rendered as a line drawing, in accordance with the code attached to the
   various control points; and the processed data is then converted into a
   form which is appropriate for scan conversion.
ABSTRACT WORD COUNT: 217

LEGAL STATUS (Type, Pub Date, Kind, Text):

```
Application:        850626 A2 Published application (A1with Search Report
                              ;A2without Search Report)
Change:             850710 A2 Title of invention (German) (change)
Change:             850710 A2 Title of invention (French) (change)
Change:             861203 A2 Representative (change)
Search Report:      871119 A3 Separate publication of the European or
                              International search report
Examination:        880720 A2 Date of filing of request for examination:
                              880516
Change:             881019 A2 Representative (change)
*Assignee:          881019 A2 Applicant (transfer of rights) (change):
                              BTS-BROADCAST TELEVISION SYSTEMS, INC.
                              (1007030) P.O. Box 30816, 2300 South 2300 West
                              Salt Lake City Utah 84131 (US) (applicant
                              designated states: DE;FR;GB;IT)
*Assignee:          881019 A2 Previous applicant in case of transfer of
                              rights (change): Robert Bosch Corporation
                              (643590) P.O. Box 31816 2300 South 2300 West
                              Salt Lake City Utah 84131 (US) (applicant
                              designated states: DE;FR;GB;IT)
Change:             881214 A2 Representative (change)
Change:             890208 A2 Representative (change)
Examination:        900117 A2 Date of despatch of first examination report:
                              891205`
Withdrawal:         901010 A2 Date on which the European patent application
                              was deemed to be withdrawn: 900416
LANGUAGE (Publication,Procedural,Application): English; English; English
```

27/5/26   (Item 1 from file: 349)
DIALOG(R)File 349:PCT Fulltext
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00647120
**COMMUNICATION SYSTEM AND METHOD OF SENDING MESSAGES IN A COMMUNICATION
    SYSTEM**
**SYSTEME DE COMMUNICATIONS ET PROCEDE D'ENVOI DE MESSAGES DANS UN SYSTEME DE
    COMMUNICATIONS**
Patent Applicant/Assignee:
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    ERICSSON (publ), S-126 25 Stockholm, SE
Inventor(s):
  VASELL Jesper; Address - VASELL, Jesper, Sten Sturegatan 4, S-411 39
    Goteborg, SE
Patent and Priority Information (Country, Number, Date):
  Patent: **WO 9930456** A2 19990617
  Application: WO 98SE2177 19981130 (PCT/WO SE9802177)
  Priority Application: SE 974565 19971208
Designated States: AL; AM; AT; AU; AZ; BA; BB; BG; BR; BY; CA; CH; CN; CU;
  CZ; DE; DK; EE; ES; FI; GB; GD; GE; GH; GM; HR; HU; ID; IL; IS; JP; KE;
  KG; KP; KR; KZ; LC; LK; LR; LS; LT; LU; LV; MD; MG; MK; MN; MW; MX; NO;
  NZ; PL; PT; RO; RU; SD; SE; SG; SI; SK; SL; TJ; TM; TR; TT; UA; UG; UZ;
  VN; YU; ZW; GH; GM; KE; LS; MW; SD; SZ; UG; ZW; AM; AZ; BY; KG; KZ; MD;
  RU; TJ; TM; AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LU; MC;
  NL; PT; SE; BF; BJ; CF; CG; CI; CM; GA; GN; GW; ML; MR; NE; SN; TD; TG
Main International Patent Class: H04L-000/;
Publication Language: English
Filing Language: English
Fulltext Availability:
  Detailed Description
  Claims
Fulltext Word Count: 9073

English Abstract
  A distributed communication system comprising a number of nodes,
  comprising a number of resources, which nodes are interconnected by an
  interconnection network. Distributed applications are executed through
  sending messages between resources in said nodes. The resources are
  categorized into a number of function types wherein resources grouped
  into one and the same function type are functionally equivalent at least
  to a given extent so that a number of function type instances are
  provided for each function type. Each node comprises information holding
  means (11) keeping information about which function type instances
  correspond to a given function type and distribution functions (12)
  associated with said information holding means (11) for selecting a
  receiving function type instance among the available instances. A
  resource sending a message only has to give the function type as address
  information and the distribution function (12) selects which function
  type instance will be the receiver.

French Abstract
  L'invention concerne un systeme de communications reparti comprenant un
  certain nombre de noeuds. Ces noeuds contiennent un certain nombre de
  ressources et sont interconnectes par un reseau d'interconnexion. Les
  applications reparties sont executees par l'envoi de messages entres les
  ressources desdits noeuds. Les ressources sont classees par types de
  fonctions, les ressources regroupees dans un seul et meme type de
  fonction etant au moins dans une certaine mesure fonctionnellement
  equivalentes, de telle facon qu'un certain nombre d'instances de types de
  fonctions soient fournies pour chaque type de fonction. Chaque noeud
  comporte des moyens de fonds d'informations (11) permettant de conserver
  des informations sur les differentes instances correspondant a un type de
  fonction donne et des fonctions reparties (12) associees a ces moyens de
  fonds d'informations (11) et permettant de selectionner parmi les
  instances disponibles une instance d'un type de fonction de reception.
  Une ressource envoyant un seul message doit donner le type de fonction
  comme information d'adresse et la fonction de repartition (12)
  selectionne l'instance du type de fonction qui sera receptrice.

 27/5/27   (Item 2 from file: 349)
DIALOG(R)File 349:PCT Fulltext
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00298383
**SIMULTANEOUS   DATA-DRIVEN   AND   DEMAND-DRIVEN   COMPUTATIONAL   MODEL   FOR
   DYNAMICALLY CONFIGURED SYSTEMS**
**MODELE   DE CALCUL ARTICULE SIMULTANEMENT AUTOUR DE LA BASE DE DONNEES ET DE
   LA DEMANDE DESTINE A DES SYSTEMES CONFIGURES DE MANIERE DYNAMIQUE**
Patent Applicant/Assignee:
  VANDERBILT UNIVERSITY
Inventor(s):
  SZTIPANOVITS Janos
  BIEGL Csaba
  KARSAI Gabor
Patent and Priority Information (Country, Number, Date):
  Patent: **WO 9208196** A1 19920514
  Application: WO 91US7397 19911007 (PCT/WO US9107397)
  Priority Application: US 90602961 19901024
Designated States: AT; AU; BE; CA; CH; DE; DK; ES; FR; GB; GR; IT; JP; LU;
  NL; SE
Main International Patent Class: G06F-013/14;
Publication Language: English
Fulltext Availability:

Detailed Description
Claims
Fulltext Word Count: 4898

English Abstract
In a model-based dynamically configured system (15, 25), various
processing components (65, 75, 87) are created dynamically, interfaced to
each other, and scheduled upon demand. A combination of data driven and
demand-driven scheduling techniques (Fig. 5, 6) are used to enhance the
effectiveness of the dynamically configured system.

French Abstract
Dans un systeme configure de maniere dynamique fonde sur un modele (15,
25), plusieurs elements de traitement (65, 75, 87) sont crees
dynamiquement, relies les uns aux autres, et organises en fonction de la
demande. Un melange de techniques d'organisation (Fig. 5, 6) articulees
autour de la base de donnees et de la demande sont utilisees pour
accroitre l'efficacite du systeme configure de maniere dynamique.

27/5/28   (Item 3 from file: 349)
DIALOG(R)File 349:PCT Fulltext
(c) 2000 WIPO/MicroPatent. All rts. reserv.

00269230
**PARALLEL DISTRIBUTED PROCESSING NETWORK CHARACTERIZED BY AN INFORMATION
   STORAGE MATRIX**
**RESEAU DE TRAITEMENT REPARTI PARALLELEMENT ET CARACTERISE PAR UNE MATRICE
   DE STOCKAGE D'INFORMATIONS**
Patent Applicant/Assignee:
  EI DU PONT DE NEMOURS AND COMPANY
Inventor(s):
  SAMARDZIJA Nikola
Patent and Priority Information (Country, Number, Date):
  Patent: **WO 9015390** A1 19901213
  Application: WO 90US2699 19900521   (PCT/WO US9002699)
  Priority Application: US 89360804 19890602
Designated States: AT; BE; CH; DE; DK; ES; FR; GB; IT; JP; LU; NL; SE
Main International Patent Class: G06F-015/18;
Publication Language: English
Fulltext Availability:
  Detailed Description
  Claims
Fulltext Word Count: 9713
English Abstract
  A single layer parallel distributed processing network (10) is
  characterized by having connection weights between nodes that are defined
  by an [N x N] information storage matrix (A) that satisfies the matrix
  equation: [A] [T] = [T] [LAMBDA], where [LAMBDA] is an [N x N] diagonal
  matrix the components of which are the eigenvalues of the matrix [A] and
  [T] is an [N x N] similarity transformation matrix whose columns are
  formed of some predetermined number M of target vectors (where M < = N)
  and whose remaining columns are formed of some predetermined number Q of
  slack vectors (where Q = N - M), both of which together comprise the
  eigenvectors of [A].

French Abstract
  Un reseau monocouche de traitement reparti parallelement (10) est
  caracterise en ce qu'il comporte des priorites de connexion entre les
  noeuds qui sont definies par une (N x N) matrice de stockage
  d'informations (A) qui repond a l'equation matricielle: (A) (T) = (T)
  (LAMBDA), ou (LAMBDA) est une (N x N) matrice diagonale dont les

composantes sont les valeurs propres de la matrice (A) et (T) est une (N x N) matrice de transformation par similitude dont les colonnes sont formees d'un nombre predetermine M de vecteurs cibles (ou M < = N) et dont les colonnes restantes sont formees d'un nombre predetermine Q de vecteurs de remplissage (ou Q = N - M), les deux constituant ensemble les vecteurs propres de (A).

27/5/29   (Item 4 from file: 349)
DIALOG(R)File 349:PCT Fulltext
(c) 2000 WIPO/MicroPatent. All rts. reserv.

00242744
HIGH PERFORMANCE GRAPHICS WORKSTATION
POSTE DE TRAVAIL GRAPHIQUE A HAUTE PERFORMANCE
Patent Applicant/Assignee:
  DIGITAL EQUIPMENT CORPORATION
Inventor(s):
  DOYLE Peter Lawrence
  ELLENBERGER John Philipp
  JONES Ellis Olivier
  CARVER David C
  DIPIRRO Steven D
  GEROVAC Branko J
  ARMSTRONG William Paul
  GIBSON Ellen Sarah
  SHAPIRO Raymond Elliott
  RUSHFORTH Kevin C
  ROACH William C
Patent and Priority Information (Country, Number, Date):
  Patent: **WO 8901664** A1 19890223
  Application: WO 88US2727 19880812   (PCT/WO US8802727)
  Priority Application: US 8785081 19870813
Designated States: AT; BE; CH; DE; FR; GB; IT; JP; LU; NL; SE
Main International Patent Class: G06F-012/02;
International Patent Class: G06F-003/153;
Publication Language: English
Fulltext Availability:
  Detailed Description
  Claims
Fulltext Word Count: 25645

English Abstract
  A high performance graphics workstation includes a digital computer host and a graphics subsystem. Two- and three-dimensional graphics data structures, built by the host, are stored in the graphics subsystem. The asynchronous traversal of the data structures together with traversal control functions coordinate and control the flow of graphics data and commands to a graphics pipeline for processing and display. The address space of the graphics subsystem is mapped into a reversed I/0 space of the host. This permits the host to directly access the graphics subsystem.

French Abstract
  Un poste de travail graphique a haute performance comprend un ordinateur central numerique et un sous-systeme graphique. Des structures de donnees graphiques bi-dimensionnelles et tri- dimensionnelles, construites par l'ordinateur central, sont stockees dans le sous-systeme graphique. Le parcours asynchrone des structures de donnees avec les fonctions de commande du parcours coordonnent et commandent le flux des donnees graphiques et des instructions vers un pipeline de donnees graphiques a des fins de traitement et d'affichage. L'espace d'adresse du sous-systeme

graphique est topographie dans un espace I/0 inverse de l'ordinateur central. Ceci permet a l'ordinateur central d'avoir un acces direct au sous-systeme graphique.

27/5/30   (Item 5 from file: 349)
DIALOG(R)File 349:PCT Fulltext
(c) 2000 WIPO/MicroPatent. All rts. reserv.

00231350
DATAFLOW PROCESSING ELEMENT, MULTIPROCESSOR, AND PROCESSES
ELEMENT DE TRAITEMENT DE FLUX DE DONNEES, MULTIPROCESSEUR ET PROCEDES
Patent Applicant/Assignee:
  DENNIS Jack B
Inventor(s):
  DENNIS Jack B
Patent and Priority Information (Country, Number, Date):
  Patent: **WO 8800732** A1 19880128
  Application: WO 87US1668 19870713 (PCT/WO US8701668)
  Priority Application: US 86885836 19860715
Designated States: AU; BE; CH; DE; FR; GB; IT; JP; NL; SE
Main International Patent Class: G06F-003/00;
International Patent Class: G06F-009/30; G06F-009/36; G06F-009/38;
  G06F-009/40; G06F-013/00;
Publication Language: English
Fulltext Availability:
  Detailed Description
  Claims
Fulltext Word Count: 15692

English Abstract
  A novel computer design that is capable of utilizing large numbers of very large scale integrated (VLSI) circuit chips as a basis for efficient high performance computation. This design is a static dataflow architecture of the type in which a plurality of data flow processing elements (110) communicate externally by means of input/output circuitry (128), and internally by means of packets sent through a routing network (124) via paths (122). The routing network (124) implements a transmission path from any processing element to any other processing element. This design effects processing element transactions on data according to a distribution of instructions that is at most partially ordered. These instructions correspond to the nodes of a directed graph in which any pair of nodes connected by an arc corresponds to a predecessor-successor pair of instructions. Generally each predecessor instruction has one or more successor instructions, and each successor instruction has one or more predecessor instructions. In accordance with the present invention, these instructions include associations of execution components and enable components identified by instruction indices. Un ordinateur ayant une conception novatrice peut utiliser de grandes quantites de plaquettes a circuits integres a tres grande echelle (VLSI) comme base efficace de calcul a tres haute performance. Cette conception est une architecture a flux statique de donnees du type ou une pluralite d'elements de traitement de flux de donnees (110) communiquent exterieurement par des circuits d'entree/sortie (128) et interieurement par des paquets envoyes par un reseau d'acheminement (124) via des parcours (122). Le reseau d'acheminement (124) met en oeuvre des parcours de transmission de n'importe quel element de traitement a n'importe quel autre element de traitement. Cette configuration effectue des transactions de donnees entre elements de traitement selon des instructions distribuees de facon tout au plus partiellement ordonnee. Ces instructions correspondent aux points nodaux d'un graphique de directions dans lequel toute paire de points nodaux relies par un arc correspond a une paire d'instructions predecesseur-successeur. En

general, chaque instruction predecesseur a une ou plusieurs instructions successeur et chaque instruction successeur a une ou plusieurs instructions predecesseur. Ces instructions font intervenir des associations de composants d'execution et de composants de validation identifies par des indices d'instruction.

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*    Cover Sheet                                                              *
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     ***  Your Memo ***
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*                                                                             *
*    Prepared for: Examiner Zhen                                              *
*                                                                             *
*    By          : Ginger Roberts                                            *
*                                                                             *
*    Date        : May 10, 2000                                              *
*                                                                             *
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Attached please for the results of your search for 08/997142. The search
was conducted on Dialog which includes IEEE, Computer Databases, and
Worldwide Patents.

The following additional products were also searched: --

Please let me know if you need any further information regarding the search
or if you would like to enhance the search strategy in any way.

Thank you for using the Electronic Information Center.

Sincerely,

Ginger D. Roberts
Technical Information Specialist
308-7795

Please review all hits - especially high tech literature

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File 351:DERWENT WPI 1963-2000/UD=, UM=, & UP=200022
        (c) 2000 Derwent Info Ltd
File 344:Chinese Patents ABS Apr 1985-2000/Feb
        (c) 2000 European Patent Office
File 347:JAPIO Oct 1976-1999/Oct(UPDATED 000208)
        (c) 2000 JPO & JAPIO

Set	Items	Description
S1	16360	(PARALLEL OR PIPELINE OR ARRAY OR VECTOR OR CONCURRENT? OR SIMULTANEOUS?)(2N)(PROCESSOR? ? OR PROCESSING OR SERVER)
S2	358	HYPERCUBE? ? OR HYPER()CUBE? ? OR SMP OR MPP
S3	4085	MC=(T01-M02C? OR T01-F03B?)
S4	25966	IC=G06F-015/16
S5	1180869	CAPACITY OR PERFORMANCE OR LOAD OR EXECUT?(2N)TIME? ? OR R-ESOURCE? ? OR THROUGHPUT OR THROUGH()PUT OR TRAFFIC OR CONCUR-RENCY OR BOTTLENECK? ? OR TRACE()TOOL? ? OR STATISTIC? ? OR W-ORKLOAD OR CLUSTER(2N)MANAG? OR DATA()HANDLING
S6	1335853	GRAPH? OR VISUAL? OR PICTORIAL OR PICTURE OR 3()D OR THREE-()DIMENSIONAL OR 3D OR IMAGE OR IMAGES OR ILLUSTRATION OR X()Y OR XY OR MATRIX OR MATRICES
S7	244753	NODE OR NODES OR VERTEX OR VERTICES OR CORNER OR TRIANGULAR OR TRIANGLE? ? OR CROSS()POINT? ? OR CROSSPOINT? ? OR FORK? ?
S8	42428	S1:S4
S9	76	S5 AND S6 AND S7 AND S8
S10	2	S9 AND PR=19980101:99999999
S11	0	S9 AND PR=980101:999999
S12	2	S9 AND PR=19980101:20000510
S13	2	S10 OR S12
S14	74	S9 NOT S13

?t14/5/all

14/5/1   (Item 1 from file: 351)
DIALOG(R)File 351:DERWENT WPI
(c) 2000 Derwent Info Ltd. All rts. reserv.

012662379   **Image available**
WPI Acc No: 99-468484/199939
XRPX Acc No: N99-349806
Computer graphics **system**
Patent Assignee: HEWLETT-PACKARD CO (HEWP)
Inventor: KRECH A S; RENTSCHLER E; SCOTT N D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
US 5940086	A	19990817	US 97781671	A	19970110	G06F-015/16	199939 B

Priority Applications (No Type Date): US 97781671 A 19970110
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
US 5940086	A		18			

Abstract (Basic): US 5940086 A
        NOVELTY - A distributor (118) dynamically allocates each of the
    chunks of the **vertex** data to one of geometry accelerators (120) to
    provide a corresponding chunk of the rendering data. The allocation is
    based on the relative capability of the accelerators to process the
    vertex data. The relative processing capability is identified based on
    status information provided by accelerators.
        DETAILED DESCRIPTION - Several geometry accelerators (120) are
    configured to process **vertex** data representing **graphic** primitive
    and to provide rendering data. The accelerators generate availability

status information indicating various levels of **vertex** data
processing capability. The levels represent a series of successively
greater capability to process **vertex** data. An INDEPENDENT CLAIM is
also included for the method of processing **vertex** data in computer
graphics system.
    USE - For displaying **graphical** representations of objects on two
dimensional video display screen.
    ADVANTAGE - Efficient distribution of **vertex** data substantially
reduces the amount of time for which the geometry accelerators remain
idle, thereby increasing efficiency of accelerators, and overall
parallel processing of **vertex** data. Selective utilization of
geometry accelerators results in significant increase in **throughput**
of **graphic** system.
    DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of
the computer **graphics** system.
    Distributor (118)
    Geometry accelerators (120)
    pp; 18 DwgNo 1/5
Title Terms: COMPUTER; **GRAPHIC** ; SYSTEM
Derwent Class: T01
International Patent Class (Main): **G06F-015/16**
File Segment: EPI

 14/5/2   **(Item 2 from file: 351)**
DIALOG(R)File 351:DERWENT WPI
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012651422   **Image available**
WPI Acc No: 99-457527/199938
Related WPI Acc No: 91-094519
XRPX Acc No: N99-384587
   Parallel processing **for general purpose multiple instruction multiple
data computer systems - None**
Patent Assignee: SANDIA CORP (SAND-N)
Inventor: BENNER R E; GUSTAFSON J L; MONTRY G R
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date   Applicat No Kind Date   Main IPC   Week
US 5935216 A 19990810 US 89317389 A 19890301 G06F-015/163 199938 B
                 US 91748736 A 19910822

Priority Applications (No Type Date): US 89317389 A 19890301; US 91748736 A
  19910822
Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
US 5935216 A   24 Div ex   US 89317389
                Div ex   US 5072371
Abstract (Basic): US 5935216 A
    NOVELTY - The method involves writing messages to each neighboring
processor, in the fore and aft order to overlap the startup, copy and
transfer time of further messages with the transfer time of previous
the message.
    DETAILED DESCRIPTION - The messages are read from each of the
neighboring processors in reverse order to the orientation to overlap
the startup and transfer time with the copy of the last message.
Readings are performed until all selected processors are read. The
computation time of specific processor **nodes** can be computed using a
FORTRAN compiler and memory to memory operations.
    USE - For use in general purpose MIMD computer systems.
    ADVANTAGE - Ensures efficient and time saving communication between
processors, input and output devices using **parallel processing**

methods. Avoids dynamic reconfiguration or **load** balancing by
allocation of work assignments and combines data into single messages
where possible this also reduces the number of synchronized to reduce
synchronization costs to **performance** .
     DESCRIPTION OF DRAWING(S) - The figure shows the **graphic**
representation of a parallel computing system.
     Dwg.14/15
Title Terms: PARALLEL; PROCESS; GENERAL; PURPOSE; MULTIPLE; INSTRUCTION;
  MULTIPLE; DATA; COMPUTER; SYSTEM
Derwent Class: T01
International Patent Class (Main): G06F-015/163
File Segment: EPI

 14/5/3   (Item 3 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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012579580   **Image available**
WPI Acc No: 99-385687/199932
XRPX Acc No: N99-288802
 Sending messages in communication system
Patent Assignee: TELEFONAKTIEBOLAGET ERICSSON L M (TELF)
Inventor: VASELL J
Number of Countries: 082 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
WO 9930456	A2	19990617	WO 98SE2177	A	19981130	H04L-000/00	199932 B
SE 9704565	A	19990609	SE 974565	A	19971208	G06F-015/16	199935
SE 511098	C2	19990802	SE 974565	A	19971208	G06F-009/46	199937
AU 9917909	A	19990628	AU 9917909	A	19981130	H04L-000/00	199946

Priority Applications (No Type Date): SE 974565 A 19971208
Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
WO 9930456 A2 E 45
   Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU
   CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK
   LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ
   TM TR TT UA UG UZ VN YU ZW
   Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR
   IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW
AU 9917909 A   Based on   WO 9930456

Abstract (Basic): WO 9930456 A2
     NOVELTY - If a **resource** of the kind thread (T10) wants to send a
message (MSG), it is given as a function type (F10) of the receiver
and, in an information holding means (11), function types (T20,T30,T40)
are instances of the function type F10. A distribution function (12)
performs the actual choice of a receiving entity and chooses from the
currently available function type instances. The selected message is
then sent to T30 for instance
     DETAILED DESCRIPTION - Independent claims are included for a
distributed communication system, for a **node** in such a system and for
a method of providing communications among applications
     USE - Sending messages in distributed communication system
     ADVANTAGE - Enabling use of newly added **nodes** or **resources** and
handling removal of **nodes** or **resources**
     DESCRIPTION OF DRAWING(S) - The drawing is a simplified
 illustration of sending of message according to the invention
     Thread (T10)
     Message (MSG)

Function type (F10)
Information holding means (11)
Distribution function (12)
pp; 45 DwgNo 2/9
Title Terms: SEND; MESSAGE; COMMUNICATE; SYSTEM
Derwent Class: W01
International Patent Class (Main): G06F-009/46; **G06F-015/16** ; H04L-000/00
International Patent Class (Additional): G06F-009/46
File Segment: EPI

14/5/4   (Item 4 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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012435277   **Image available**
WPI Acc No: 99-241385/199920
XRPX Acc No: N99-331736
 Supplementary cooking apparatus for a microwave oven
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU); UNIV MINNESOTA (MINU
)
Inventor: KONG J S; LEE G H   .
Number of Countries: 002 Number of Patents: 002
Patent Family:
Patent No Kind Date   Applicat No Kind Date   Main IPC   Week
US 5937431 A   19990810 US 96679082 A   19960712 G06F-012/12   199938
KR 98010819 A   19980430 KR 9727601   A   19970626 G06F-015/16   199920 B T

Priority Applications (No Type Date): US 96679082 A 19960712
Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
US 5937431 A   18

Abstract (Basic): US 5937431 A
     NOVELTY - A dynamic memory DM cache is utilized in each **node** of a
shared memory as a backing store for data blocks discarded from the
processor cache. The address binding to the DM is delayed from the
block incoming time until the block discarding time when the blocks are
discarded from the processor cache.
     DETAILED DESCRIPTION - The processor cache stores an address tag, a
state of the block identifier, a local-global identifier and a data
block. The DM cache stores an address, the state of the block
identifier and a data block.
     USE - For data processing apparatus having memory access
architecture.
     ADVANTAGE - Delays address binding to eliminate inclusion property
between processor cache and local memory and to allow faster data
access by avoiding cache only memory architecture COMA reliance on
local memory as larger higher-level cache for processor cache. Can
create more usable local memory space and reduce memory overhead,
thereby allowing improvement in **performance** of distributed shared
memory DSM architecture.
     DESCRIPTION OF DRAWING(S) - The drawing shows the **illustration** of
the memory access mechanism in a dynamic memory architecture DYMA
system.
     Dwg.2/9
Title Terms: SUPPLEMENTARY; COOK; APPARATUS; MICROWAVE; OVEN
Derwent Class: T01
International Patent Class (Main): G06F-012/12; **G06F-015/16**
File Segment: EPI

14/5/5   (Item 5 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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012151041   **Image available**
WPI Acc No: 98-567953/199848
XRPX Acc No: N98-441842
 Computer graphics **system for processing geometric** image **data - has
 several geometry accelerators for** parallel   processing **of** vertex
 data into chunks of rendering data, for concentration and rasterising
Patent Assignee: HEWLETT-PACKARD CO (HEWP   )
Inventor: HANDGEN E A; KRECH A S; MATTHEWS M A; RENTSCHLER E M; SHAH M S
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date   Applicat No Kind Date   Main IPC   Week
US 5821950 A   19981013 US 96634458 A   19960418 G06F-015/80   199848 B

Priority Applications (No Type Date): US 96634458 A 19960418
Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
US 5821950 A   14

Abstract (Basic): US 5821950 A
      The system includes a number of geometry accelerators (32a-c) for
  processing **vertex** data, representative of **graphics** primitives, and
  providing rendering data. A distributor (30) is provided, which is
  responsive to a **vertex** data stream, for distributing chunks of the
 vertex data to the geometry accelerators, to provide chunks of
  rendering data. The distributor generates an end of chunk bit at the
  end of a corresponding chunk of **vertex** data and distributes each end
  of chunk bit to a geometry accelerators with the corresponding chunk of
 vertex data. Each geometry accelerator transmits each end of chunk
  bit from its input to its output.

      The system also includes a concentrator (36) for receiving the
  chunks of rendering data and end of chunk bits from each geometry
  accelerator, and combining chunks of rendering data into a stream of
  rendering data, in response to an end of chunk bit. The stream of
  rendering data and stream of **vertex** data represent sequences of
 graphics primitives having the same order. The system has a rasterizer
  (46), responsive to the rendering data stream, for generating pixel
  data representative of a **graphics** display.
      ADVANTAGE - Achieves enhanced **performance** through use of
 parallel processors . Order of primitives are not changed in the
 parallel processing hardware.
      Dwg.1/6
Title Terms: COMPUTER; **GRAPHIC** ; SYSTEM; PROCESS; GEOMETRY; **IMAGE** ; DATA;
  GEOMETRY; ACCELERATE; PARALLEL; PROCESS; **VERTEX** ; DATA; CHUNK; RENDER;
  DATA; CONCENTRATE
Derwent Class: T01
International Patent Class (Main): G06F-015/80
File Segment: EPI

14/5/6   (Item 6 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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011973676   **Image available**
WPI Acc No: 98-390586/199834
XRAM Acc No: C98-118194
XRPX Acc No: N98-304755

Hole inner wall monitoring apparatus for pipelines - performs image
processing of electric signal output from each receiving element
Patent Assignee: MITSUI ZOSEN KK (MITB); TERAMOTO A (TERA-I)
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week	
JP 2779713	B2	19980723	JP 91197847	A	19910807	G01V-001/40	199834	B
JP 5039698	A	19930219	JP 91197847	A	19910807	G01V-001/40	199834	

Priority Applications (No Type Date): JP 91197847 A 19910807
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
JP 2779713	B2		8	Previous Publ.		JP 5039698

Abstract (Basic): JP 2779713 B
        The apparatus has a number of receiving elements which are arranged
    in the form of an array inside a bore-hole (2) drilled under a ground
    (1). An ultrasonic wave is radiated from the transmission elements.
    This ultrasonic wave is reflected by internal surface of the hole and
    is received by the receiving element. The surface of the receiving
    element array is divided in the form of **triangles** . The area of the
    triangle arranged at outer side in hole axis direction is made more
    than the area of **triangle** arranged at side direction of hole axis of
    receiving element **array** . The **image**   **processing** of an electric
    signal output from each receiving element is performed.
        ADVANTAGE - Shortens data processing time. Obtains **image** of small
    size and sufficient resolving degree.
        Dwg.1/13
Title Terms: HOLE; INNER; WALL; MONITOR; APPARATUS; PIPE; **PERFORMANCE** ;
 IMAGE ; PROCESS; ELECTRIC; SIGNAL; OUTPUT; RECEIVE; ELEMENT
Index Terms/Additional Words: **OIL** ; **PIPELINE**
Derwent Class: H01; Q49; S03
International Patent Class (Main): G01V-001/40
International Patent Class (Additional): E21B-047/024
File Segment: CPI; EPI; EngPI

 14/5/7   (Item 7 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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011971768   **Image available**
WPI Acc No: 98-388678/199834
XRPX Acc No: N98-303087
 Fading-resistant modulation method for wireless communication system -
 using time, space or frequency diversity for defined vector space using
 signal constellation points generated by orthogonal matrix **transform**
Patent Assignee: DASILVA V M (DASI-I); SOUSA E S (SOUS-I)
Inventor: DASILVA V M; SOUSA E S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week	
CA 2186688	A	19980328	CA 2186688	A	19960927	H04B-007/06	199834	B

Priority Applications (No Type Date): CA 2186688 A 19960927
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
CA 2186688	A		53			

Abstract (Basic): CA 2186688 A
        The method involves provision of an L-dimensional signalling
    constellation formed from Q points. Each point represents a vector in a

vector space which has L orthogonal axes. Any two of the constellation points are vectors which differ in a number of their components. Each of the L components is transmitted over either L different antennae, L different carrier frequencies or L different time slots. The signalling constellation is obtained by applying an orthogonal transformation to an L-dimensional **hypercube** , with the constellation points being its **vertices** .

The transformation preserves Euclidean distances between the signalling constellation points and the signals corresponding to the signalling constellation components transmitted in each antenna, carrier frequency or time slot are differentially encoded.

USE - E.g. digital cellular GSM.

ADVANTAGE - Diversity provides high quality operation without reduction in spectral efficiency for Rayleigh fading. Mitigates power variations to reduce probability of errors in channel. Bandwidth efficient. Provides good **performance** when coding is ineffective due to slow fading. Has significant energy savings for given bit error rate when background white Gaussian noise is present.

Dwg.1/9

Title Terms: FADE; RESISTANCE; MODULATE; METHOD; WIRELESS; COMMUNICATE; SYSTEM; TIME; SPACE; FREQUENCY; DIVERSE; DEFINE; VECTOR; SPACE; SIGNAL; POINT; GENERATE; ORTHOGONAL; **MATRIX** ; TRANSFORM
Derwent Class: W01; W02
International Patent Class (Main): H04B-007/06
File Segment: EPI

14/5/8   (Item 8 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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011846560   **Image available**
WPI Acc No: 98-263470/199824
Related WPI Acc No: 98-263471
XRPX Acc No: N98-207751
 Target program loop statement optimising - determining control omega value for iterative construct and converting def into data constraint using control omega value
Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: BEYLIN B; SUBRAMANIAN K
Number of Countries: 026 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week	
EP 843257	A2	19980520	EP 97309064	A	19971111	G06F-009/45	199824	B
JP 10161884	A	19980619	JP 97318777	A	19971119	G06F-009/45	199835	
US 5930510	A	19990727	US 96752683	A	19961119	G06F-009/44	199936	

Priority Applications (No Type Date): US 96752683 A 19961119
Cited Patents: No-SR.Pub
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
EP 843257	A2	E	21			

    Designated States (Regional): AL AT BE CH DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

JP 10161884	A		26			

Abstract (Basic): EP 843257 A
The method involves use of loop statement having characteristics of a single basic block loop. It requires detecting that the loop statement contains at least one body statement that results in a def of an unspillable **resource** . A control omega value is determined for the iterative construct. The def is converted into a data constraint using

the control omega value. The iterative construct is then scheduled.
   The method further entails allocating the unspillable **resource**
dependent on the data constraint. The unspillable **resource** may be a
predicate register. The loop statement results in a data dependency
graph , the def is represented by a def **node** in the data dependency
graph . During converting, it entails adding a self output arc to the
def **node** , and assigning the control omega value to the self output
arc.
   USE - For optimising order of computer operation codes resulting
from compilation of program loop.
   ADVANTAGE - Allows optimising single basic block loop within target
program, thus, permits two or more instructions to be issued in single
clock cycle within computer structure.
   Dwg.4/7
Title Terms: TARGET; PROGRAM; LOOP; STATEMENT; OPTIMUM; DETERMINE; CONTROL;
  OMEGA; VALUE; ITERATIVE; CONSTRUCTION; CONVERT; DATA; CONSTRAIN; CONTROL;
  OMEGA; VALUE
Derwent Class: T01
International Patent Class (Main): G06F-009/44; G06F-009/45
International Patent Class (Additional): G06F-009/38
File Segment: EPI

 14/5/9   (Item 9 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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011827082   **Image available**
WPI Acc No: 98-243992/199822
XRPX Acc No: N98-193105
 Multimedia image **processing system for large scale** parallel array
  processor **e.g. supercomputer - comprises multiple processor arrays by**
 which different applications is performed in parallel manner
Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: DELGADO-FRIAS J G; PECHANEK G G; VASSILIADIS S
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
JP 8171537	A	19960702	JP 93128714	A	19930531	G06F-015/16	199822 B
US 6041398	A	20000321	US 92904916	A	19920626	G06F-015/80	200021

Priority Applications (No Type Date): US 92904916 A 19920626
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
JP 8171537	A		94			

Abstract (Basic): JP 8171537 A
   The system comprises multiple processing units which are coupled
together in the form of a **processor** **array** . Several **processor**
arrays are connected repeatedly to form a processor mesh.
   By the frequency division multiplexing technique, the general
purpose applications such as multimedia applications are performed by a
specific **processor** **array** and other applications are performed in
parallel by the other **processor** **array** .
   ADVANTAGE - Enables easy modification of processor mesh. Increases
number of **node** connections between processors. Enables maintenance of
processing function easily.
   Dwg.1/75
Title Terms: **IMAGE** ; PROCESS; SYSTEM; SCALE; PARALLEL; ARRAY; PROCESSOR;
  COMPRISE; MULTIPLE; PROCESSOR; ARRAY; APPLY; **PERFORMANCE** ; PARALLEL;
  MANNER
Derwent Class: T01

International Patent Class (Main): **G06F-015/16** ; G06F-015/80
File Segment: EPI

 14/5/10   (Item 10 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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011813232   **Image available**
WPI Acc No: 98-230142/199820
XRPX Acc No: N98-182292
 N-dimensional parallel **seismic data** processing **method - involves
 allocating processors as host** node **and worker** nodes **which are
 assigned in parallel to data divided into depth slices in memory**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: ROBINSON B R
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date   Applicat No Kind Date   Main IPC   Week
US 5734829 A 19980331 US 95546204 A 19951020 G06F-017/00   199820 B

Priority Applications (No Type Date): US 95546204 A 19951020
Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
US 5734829 A   13

Abstract (Basic): US 5734829 A
      The data processing method involves allocating one of the
  processors of the **parallel** computer system as a host **node** for
   distributing the data. Multiple processors are allocated as worker
  nodes for processing the data in parallel. The data is divided into
   slices along one of the dimensions of the data representing depth. Each
   slice is distributed to memory segments of the distributed memory.
      Each worker **node** is assigned to memory segments of the
   distributed memory to which a slice has been assigned, such that
   contiguous slices are assigned to different worker **nodes** . Each worker
  node processes a slice in parallel with and independent from the
   slices being processed by other worker **nodes** . The worker **nodes** are
   assigned to balance the **load** of processing the data among the worker
  nodes .
      ADVANTAGE - Allows routine application of sophisticated **3D** DMO
   processes. Can handle arbitrarily irregular surveys.
      Dwg.8/8
Title Terms: N; DIMENSION; PARALLEL; SEISMIC; DATA; PROCESS; METHOD;
  ALLOCATE; PROCESSOR; HOST; **NODE** ; WORK; **NODE** ; ASSIGN; PARALLEL; DATA;
  DIVIDE; DEPTH; SLICE; MEMORY
Index Terms/Additional Words: **DIP** ; **MOVE** ; OUT
Derwent Class: S03; T01
International Patent Class (Main): G06F-017/00
File Segment: EPI

 14/5/11   (Item 11 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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011786094   **Image available**
WPI Acc No: 98-203004/199818
XRPX Acc No: N98-161714
 **Synchronous serial data processing computer in high speed packet
 switching system,** graphic **patterning apparatus - performs sequential
 processing to each bit input data which is serially forwarded between set**

of nodes **through switching network**
Patent Assignee: SHIMAZU H (SHIM-I)
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date   Applicat No Kind Date   Main IPC   Week
JP 10055350 A 19980224 JP 96243961 A 19960812 G06F-015/82   199818 B

Priority Applications (No Type Date): JP 96243961 A 19960812
Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
JP 10055350 A   5

Abstract (Basic): JP 10055350 A
      The computer has a switching network (1) which is connected with a
   serial input-output integer adder and multiplier (2,3). A serial input
   integer judgment **node** (4), switch **node** (5) and a register **node**
   (6) are also connected with the switching network.
      Serial forwarding of data is carried out between the **nodes** , which
   are connected by a single wiring, through the switching network.
   Sequential process is carried out to each bit of the input data.
      ADVANTAGE - Simplifies wiring between **nodes** . Decreases amount of
   hardware required. Attains various **parallel   processing** easily.
      Dwg.1/8
Title Terms: SYNCHRONOUS; SERIAL; DATA; PROCESS; COMPUTER; HIGH; SPEED;
   PACKET; SWITCH; SYSTEM; **GRAPHIC** ; PATTERN; APPARATUS; **PERFORMANCE** ;
   SEQUENCE; PROCESS; BIT; INPUT; DATA; SERIAL; FORWARDING; SET; **NODE** ;
   THROUGH; SWITCH; NETWORK
Derwent Class: T01
International Patent Class (Main): G06F-015/82
File Segment: EPI

 14/5/12   (Item 12 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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011748319   **Image available**
WPI Acc No: 98-165229/199815
XRPX Acc No: N98-131712
   Three   dimensional **concealed** graphical **surface elimination**
 processing device for high speed image **processing - has geometrical**
 processing unit which performs disposal of three   dimensional
  graphical **data based on output of rear surface processing unit**
Patent Assignee: SHARP KK (SHAF)
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date   Applicat No Kind Date   Main IPC   Week
JP 10031755 A 19980203 JP 96184728 A 19960715 G06T-015/40   199815 B

Priority Applications (No Type Date): JP 96184728 A 19960715
Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
JP 10031755 A   7

Abstract (Basic): JP 10031755 A
      The device has a **graphic** data memory unit (1) which stores
   vertex co-ordinate of a polygon comprising **three   dimensional**
   graphics . A modeling conversion setting unit (2) outputs a **matrix**
    data for performing coordinate transformation of **three   dimensional**
   graphic . A modeling conversion memory unit (4) stores the output of
    the modelling conversion setting unit. Projection conversion setting
    unit (3) sets the gaze vector of the perspective projection or the

parallel projection. The output of projection conversion setting unit
is stored in a projection conversion memory (5).
    Based on the contents of both the memories, a rear surface
processing unit (6) outputs a code corresponding to the product of the
normal line vector of the polygon and the gaze **vector** . A geometrical
processing unit (7) performs disposal of **three** **dimensional**
graphical data based on the output of rear surface processing unit.
    ADVANTAGE - Aims at acceleration of **image** processing by reducing
number of polygons. Improves **image** processing speed.
    Dwg.1/3
Title Terms: THREE; DIMENSION; CONCEAL; **GRAPHICAL** ; SURFACE; ELIMINATE;
  PROCESS; DEVICE; HIGH; SPEED; **IMAGE** ; PROCESS; GEOMETRY; PROCESS; UNIT;
 PERFORMANCE ; DISPOSABLE; THREE; DIMENSION; **GRAPHICAL** ; DATA; BASED;
  OUTPUT; REAR; SURFACE; PROCESS; UNIT
Derwent Class: T01
International Patent Class (Main): G06T-015/40
File Segment: EPI

 14/5/13   (Item 13 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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011718472   **Image available**
WPI Acc No: 98-135382/199813
XRPX Acc No: N98-107206
 First order equation solution obtaining method for parallel   processing
  system - involves dividing analysis area into several sub areas and
 assigning processor for every area related to shared node at
 demarcation of sub area
Patent Assignee: HITACHI LTD (HITA)
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date   Applicat No Kind Date   Main IPC   Week
JP 10011421 A   19980116 JP 96159504 A   19960620 G06F-017/12   199813 B

Priority Applications (No Type Date): JP 96159504 A 19960620
Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
JP 10011421 A   5

Abstract (Basic): JP 10011421 A
    The method involves using numerical analysis, in which a mesh is
used to calculate an area (1) for analysis. The area to be analysed is
divided into sub areas. For every sub area, a processor is assigned in
relation to a shared **node** at the demarcation of the sub area. Data
communication takes place among the processors of the sub areas.
    The data required for convergence of **matrix** calculation is shared
by all the processors. Each processor calculates the specific area
using the coefficient **matrix** and the connection demarcation
information on the divided sub areas. Thus the whole analysis area is
calculated.
    ADVANTAGE - Performs large scale analysis within short time. Avoids
need for producing **matrix** division list for every processor. Reduces
memory **capacity** and time required for calculation.
    Dwg.3/4
Title Terms: FIRST; ORDER; EQUATE; SOLUTION; OBTAIN; METHOD; PARALLEL;
  PROCESS; SYSTEM; DIVIDE; ANALYSE; AREA; SUB; AREA; ASSIGN; PROCESSOR;
  AREA; RELATED; SHARE; **NODE** ; DEMARCATION; SUB; AREA
Derwent Class: T01
International Patent Class (Main): G06F-017/12
International Patent Class (Additional): G06F-009/38

File Segment: EPI

 14/5/14   (Item 14 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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011645729   **Image available**
WPI Acc No: 98-062637/199806
XRPX Acc No: N98-049339
 MIMD modular array processor **architecture - has network interfaces**
 for linking arithmetic processors, node **memories and control**
 processors, permitting each node **to communicate with memories of other**
 nodes **for** load **balancing, buffering data and operation as high-speed**
 DMA controllers
Patent Assignee: HUGHES AIRCRAFT CO (HUGA)
Inventor: DAVIES S P; HARRISON R L
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date   Applicat No Kind Date   Main IPC   Week
US 5701482 A 19971223 US 93116432 A   19930903 G06F-015/16   199806 B
                        US 95553963 A   19951106

Priority Applications (No Type Date): US 93116432 A 19930903; US 95553963 A
   19951106
Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
US 5701482 A   9 Cont of   US 93116432

Abstract (Basic): US 5701482 A
       The modular **array processor** architecture (10) comprises
   interconnected **parallel processing nodes** (11)s that each comprise
   a control processor (12), an arithmetic processor (13) having an input
   port (22) for receiving data from an external source that is to be
   processed, a **node** memory (14) that also comprises a portion of a
   distributed global memory, and a network interface (15) coupled between
   . the control processor (12), the arithmetic processor (13), and the
    node memory (14).
       Data and control buses (17, 18) are coupled between the arithmetic
   processors (13) and network interfaces (14) of each of the processing
   nodes (11). Respective network interfaces (15) link each of the
   arithmetic processors (13), **node** memories (14) and control processors
   (12) together to provide for communication throughout the architecture
   (10) and permit each **node** to communicate with the **node** memories
   (14) of all other processing **nodes** (11). This linking, along with the
   use of a heuristic scheduling algorithm, provides for **load** balancing
   between the processing **nodes** (11). Data queues are segmented and
   distributed across the architecture (10) in a way that the source and
   destination **nodes** (11) process data locally in the memory (14), while
   overflow is kept in distributed bulk memories (14). The network
   interfaces (15) buffer data transferred over the data and control buses
   (17, 18) to a respective **node** (11). Also, the network interfaces (15)
   operate as high-speed DMA controllers to transfer data between the
   arithmetic processor (13) and **node** memory (14) of a processing **node**
   (11) independent of the operation of the control processor (12) in that
   node (11). The control bus (17) is used to keep track of available
   resources throughout the architecture (10) under control of a
   heuristic scheduling algorithm that reallocates tasks to available
   arithmetic processors (13) based on a set of heuristic rules to achieve
   the **load** balancing. The data bus (18) is used to transfer data   '
   between the **node** memories (14) so that reallocated tasks are
   performed by selected arithmetic and control processors (13, 12) using

data that is stored locally.
    USE - Can execute navy standard processing **graph** methodology.
    ADVANTAGE - High processing bandwidth. Processing and scheduling
capability grows linearly with additional **nodes** .
    Dwg.1/4
Title Terms: MODULE; ARRAY; PROCESSOR; ARCHITECTURE; NETWORK; INTERFACE;
  LINK; ARITHMETIC; PROCESSOR; **NODE** ; MEMORY; CONTROL; PROCESSOR; PERMIT;
 NODE ; COMMUNICATE; MEMORY; **NODE** ; **LOAD** ; BALANCE; BUFFER; DATA;
  OPERATE; HIGH; SPEED; DMA; CONTROL
Derwent Class: T01
International Patent Class (Main): **G06F-015/16**
International Patent Class (Additional): G06F-009/40
File Segment: EPI

 14/5/15   (Item 15 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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011498967   **Image available**
WPI Acc No: 97-476880/199744
XRPX Acc No: N97-397664
 Integral primary equation calculation method for parallel computer of
 distributed memory system - by performing elimination process for every
 row of triangular **breakdown result of coefficient** matrix **and**
 calculation result of equation right side which are both stored in
 processor memory
Patent Assignee: HITACHI LTD (HITA)
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date   Applicat No Kind Date   Main IPC   Week
JP 9223123 A   19970826 JP 9630336   A   19960219 G06F-017/12   199744 B

Priority Applications (No Type Date): JP 9630336 A 19960219
Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
JP 9223123 A   6   .

Abstract (Basic): JP 9223123 A
    The calculation method involves arranging the coefficient **matrix**
  and equation right side in a distributed memory. The equation right
  side undergoes calculated while the coefficient **matrix** undergoes a
  triangular breakdown process.
    Triangular breakdown and calculation results for every row are
  stored in the memory of a processor so that elimination process can be
  performed. The final **triangular** or calculation result is transposed
  to the other side of the equation.
    ADVANTAGE - Processor operation rate is improved by accelerating
  calculation process for equation right side.
    Dwg.1/8
Title Terms: INTEGRAL; PRIMARY; EQUATE; CALCULATE; METHOD; PARALLEL;
  COMPUTER; DISTRIBUTE; MEMORY; SYSTEM; **PERFORMANCE** ; ELIMINATE; PROCESS;
  ROW; **TRIANGLE** ; BREAKDOWN; RESULT; COEFFICIENT; **MATRIX** ; CALCULATE;
  RESULT; EQUATE; RIGHT; SIDE; STORAGE; PROCESSOR; MEMORY
Derwent Class: T01
International Patent Class (Main): G06F-017/12
International Patent Class (Additional): **G06F-015/16**
File Segment: EPI

 14/5/16   (Item 16 from file: 351)
DIALOG(R)File 351:DERWENT WPI

011286113   **Image available**
WPI Acc No: 97-264018/199724
XRPX Acc No: N97-218355
 Parallel computer system - has calculation node **and input-output** node
 provided with individual cache, which communicates with each other
 mutually
Patent Assignee: HITACHI LTD (HITA)
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date   Applicat No Kind Date   Main IPC   Week
JP 9091261 A   19970404 JP 95266474 A   19950920 G06F-015/163 199724 B

Priority Applications (No Type Date): JP 95266474 A 19950920
Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
JP 9091261 A   9

Abstract (Basic): JP 9091261 A
        The system has an array of calculation **nodes** which are connected
    in form of a **matrix** . Cache is provided at both calculation and
    input-output **nodes** . One or more cache **nodes** communicates with one
    of the input-output **nodes** through respective network. Similarly, one
    or more calculation **nodes** communicates with one of the cache **nodes** .
        Then, the calculation **node** reads the data from the secondary
    memory and a data demand message is transmitted to the cache **node** . If
    data is present in the cache, it is transmitted to the calculation
    mode. If data is not present, then it is read from secondary memory and
    is then transmitted to calculation **nodes** .
        ADVANTAGE - Reduces processing waiting time. Avoids concentration
    of processing. Improves **performance** of parallel computer.
        Dwg.1/4
Title Terms: PARALLEL; COMPUTER; SYSTEM; CALCULATE; **NODE** ; INPUT; OUTPUT;
 NODE ; INDIVIDUAL; CACHE; COMMUNICATE; MUTUAL
Derwent Class: T01
International Patent Class (Main): G06F-015/163
International Patent Class (Additional): G06F-009/46
File Segment: EPI

 14/5/17   **(Item 17 from file: 351)**
DIALOG(R)File 351:DERWENT WPI

011283683   **Image available**
WPI Acc No: 97-261588/199724
XRPX Acc No: N97-216158
 Computer network topology management and visualising **system - maintains**
 complex relationship between computer network elements to provide common
 database for storing node, **type and view data**
Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: HSU W; KULKAMI A S; KULKARNI A S
Number of Countries: 008 Number of Patents: 003
Patent Family:
Patent No Kind Date   Applicat No Kind Date   Main IPC   Week
EP 773649 A2 19970514 EP 96307993 A   19961105 H04L-012/24   199724 B
JP 9266476 A   19971007 JP 96302018 A   19961113 H04L-012/24   199750
US 5848243 A   19981208 US 95558274 A   19951113 G06F-015/16   199905

Priority Applications (No Type Date): US 95558274 A 19951113
Cited Patents: No-SR.Pub

                     14 May 10, 2000 10:16

Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
EP 773649   A2 E 35
   Designated States (Regional): DE FR GB IT NL SE
JP 9266476 A   31

Abstract (Basic): EP 773649 A
        The computer network has several network **nodes** and
    interconnections. A network management system includes a database of
    managed network **resources** . The database defines network **nodes** ,
    associated **node** types and associated views of the **nodes** . The system
    is operable to modify the views based on user input changes in
    attributes of the **nodes** . Network management users are arranged to
    display views of said network using the network management database.
        Preferably, the attributes of the **nodes** include parent
    relationships. The system is arranged to form a new view **node** each
    time a new parent is added to an attribute of a **node** . The system is
    arranged to delete a view **node** each time a parent is deleted from
    attributes of a **node** .
        USE/ADVANTAGE - Allows maintenance and viewing of physical and
    logical network topology. Enables users to access data only through
    physical topology database, with both physical and logical topology.
        Dwg.3/6
Title Terms: COMPUTER; NETWORK; TOPOLOGICAL; MANAGEMENT; **VISUAL** ; SYSTEM;
  MAINTAIN; COMPLEX; RELATED; COMPUTER; NETWORK; ELEMENT; COMMON; DATABASE;
  STORAGE; **NODE** ; TYPE; VIEW; DATA
Derwent Class: W01
International Patent Class (Main): H04L-012/24
International Patent Class (Additional): G06F-013/00; **G06F-015/16** ;
  H04L-012/26
File Segment: EPI

 14/5/18   (Item 18 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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011099247   **Image available**
WPI Acc No: 97-077172/199707
Related WPI Acc No: 98-297338
XRPX Acc No: N97-064132
 SIMD mesh parallel computer architecture for connection to host computer
 - has master processor element for broadcasting instructions to array of
 synchronous-execution slave processor elements, each contg. input-output
 processor section for routing data, and core processor
Patent Assignee: MASSACHUSETTS INST TECHNOLOGY (MASI)
Inventor: GILBERT I H
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date   Applicat No Kind Date   Main IPC   Week
US 5590356 A 19961231 US 94294757 A   19940823 G06F-013/00   199707 B

Priority Applications (No Type Date): US 94294757 A 19940823
Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
US 5590356 A   80

Abstract (Basic): US 5590356 A
        The Monolithic Synchronous Processor (Mesh-SP) processes data and
    incorporates a mesh parallel computer architecture, primarily SIMD,
    Each Mesh-SP processor **node** utilizes a single DSP processor element,
    a large internal memory of at least 128k-bytes, and separately operable

computational and I-O processing sections.
     The processor element provides data **throughput** of at least 120
MFlops. The processor is programmed in ANSI C and without parallel
extensions. A combination of on-chip DMA hardware and system software
simplifies data I-O and inter-processor communication. A functional
simulator enables Mesh-SP algorithms to be coded and tested on a
personal computer.
     USE/ADVANTAGE - Combines high data **throughput** with modest size,
weight, power and cost. Facilitates software development. Mesh-SP
appears to programmer as single computer which executes single program,
reducing programming complexity. Mesh-SP is programmed to solve wide
variety of computationally-demanding signal processing problems, e.g.
three -dimensional graphics or multi-dimensional signal processing,
neural networks, tomographic reconstruction, large Fourier transforms
and solving linear equations.
     Dwg.1/15
Title Terms: SIMD; MESH; PARALLEL; COMPUTER; ARCHITECTURE; CONNECT; HOST;
  COMPUTER; MASTER; PROCESSOR; ELEMENT; BROADCAST; INSTRUCTION; ARRAY;
  SYNCHRONOUS; EXECUTE; SLAVE; PROCESSOR; ELEMENT; CONTAIN; INPUT; OUTPUT;
  PROCESSOR; SECTION; ROUTE; DATA; CORE; PROCESSOR
Derwent Class: T01
International Patent Class (Main): G06F-013/00
File Segment: EPI

 14/5/19   (Item 19 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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011087079   **Image available**
WPI Acc No: 97-065003/199706
XRPX Acc No: N97-053550
 Multidimensional spectral load **balancing apparatus for circuit design -
 includes procedure which uses series of eigenvectors of Laplacian** matrix
 of graph **of problem to partition problem**
Patent Assignee: SANDIA CORP (SAND-N)
Inventor: HENDRICKSON B A; LELAND R W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week	
US 5587922	A	19961224	US 9378667	A	19930616	G06F-015/16	199706	B
			US 96680718	A	19960715	B		

Priority Applications (No Type Date): US 9378667 A 19930616; US 96680718 A
  19960715
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
US 5587922	A		12	Cont of	US 9378667	

Abstract (Basic): US 5587922 A
     The parallel computational apparatus includes a series of
computational units which are connected in pairs via data links. The
data links define the connection topology of the parallel computer
system. A procedure subdivides a given problem among the computational
units.
     The procedure involves constructing a **graph** which corresponds to
the given problem. The **graph** includes a series of **vertices** , which
represent a corresponding series of computational tasks of the given
problem, and a series of weighted edges which represent information
flow between the computational subtasks. A Laplacian **matrix** of the
graph is generated and k eigenvectors of the **matrix** are computed. An
orthogonal basis for a space spanned by the eigenvectors is selected.

The computational subtasks are partitioned into subsets using the eigenvectors. Each of the subsets are assigned to one of the computational units in a manner consistent with the connection topology.

USE/ADVANTAGE - Optimises **parallel** computer **processing** of problem and minimises total pathway lengths of integrated circuits in design stage.

Dwg.1/2

Title Terms: MULTIDIMENSIONAL; SPECTRAL; **LOAD** ; BALANCE; APPARATUS; CIRCUIT; DESIGN; PROCEDURE; SERIES; LAPLACE; **MATRIX** ; **GRAPH** ; PROBLEM; PARTITION; PROBLEM

Derwent Class: T01
International Patent Class (Main): **G06F-015/16**
International Patent Class (Additional): G06F-017/50
File Segment: EPI

14/5/20   (Item 20 from file: 351)
DIALOG(R)File 351:DERWENT WPI
(c) 2000 Derwent Info Ltd. All rts. reserv.

010795185   **Image available**
WPI Acc No: 96-292138/199630
XRPX Acc No: N96-245438
Coupled-vibration analysis for flow structure e.g. power, information, traffic - involves calculating compsn. matrix **on whole motion equation by** parallel **processing and analyzing combined shearing stress and viscosity**
Patent Assignee: HITACHI LTD (HITA)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week	
JP 8123852	A	19960517	JP 94264849	A	19941028	G06F-017/50	199630	B

Priority Applications (No Type Date): JP 94264849 A 19941028
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
JP 8123852	A		11			

Abstract (Basic): JP 8123852 A
The method involves seeking the **matrix** M of the couplings C, K, L1, L2, L3, L4, L5, H, D, and Q of a fluid structure by **parallel processing** . A **triangle** decomposition is done for the **matrix** M, Q, K, and H. A **matrix** operation M-1K is done on the whole motion equation and Q-1H is sought by **parallel processing** .

A process which seeks for the flow velocity is done and the flow velocity is altered. The stable critical flow velocity is computed by peculiar value calculation. The shearing stress and the influence of compression through viscosity are combined and analyzed.

ADVANTAGE - Improves analysis accuracy and shortens calculation time.

Dwg.1/6

Title Terms: COUPLE; VIBRATION; ANALYSE; FLOW; STRUCTURE; POWER; INFORMATION; **TRAFFIC** ; CALCULATE; COMPOSITION; **MATRIX** ; WHOLE; MOTION; EQUATE; PARALLEL; PROCESS; COMBINATION; SHEAR; STRESS; VISCOSITY

Derwent Class: S02; T01
International Patent Class (Main): G06F-017/50
International Patent Class (Additional): G01M-009/00
File Segment: EPI

14/5/21   (Item 21 from file: 351)

DIALOG(R)File 351:DERWENT WPI

010754453   **Image available**
WPI Acc No: 96-251408/199625
XRPX Acc No: N96-211337
 **Multi-processor operation method for PICO system - involves storing root
  nodes on expansion queue for allocation to network with nodes
  generating offsprings for routing and message broadcasts**
Patent Assignee: FMC CORP (FMCC)
Inventor: DIAMOND M D; KIMBEL J C; RENNOLET C L; ROSS S E
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
US 5517654	A	19960514	US 92888936	A	19920526	G06F-015/18	199625 B

Priority Applications (No Type Date): US 92888936 A 19920526
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
US 5517654	A		21			

Abstract (Basic): US 5517654 A
        The method involves storing a root **node** on a list of **nodes** on
     an expansion queue in a **node** generation subsystem of the PICO system.
     The expanded **nodes** are allocated to the network of multiprocessors
     and the expanded **nodes** are hashed. Offsprings are generated forming
     shadow **nodes** to occupy idle **capacity** of the network of
     multiprocessors. A message subsystem is interacted with, initialized by
     the user, to refine the shadow **nodes** . This involves routing shadow
   node offsprings via a message channel subsystem in the PICO system.
        Nodes are removed to curtail offspring generation. Bounds, values
     and upper and lower limits of the offspring are broadcast to compare
     with the root **node** and determine convergence. The broadcast is routed
     to deploy messages to the network of processors via a message channel
     subsystem in the PICO system. The PICO system is connected to the root
     processor via a state vector. Memory and shutdown operation of the PICO
     system are managed by an auxiliary function device.
        USE/ADVANTAGE - For enumerative and **graph** search problems.
     Provides near 100% processor utilisation in multiprocessor network.
     Eliminates idle process **capacity** by storing shadow **nodes** in idle
     processors.
        Dwg.4/10
Title Terms: MULTI; PROCESSOR; OPERATE; METHOD; PICO; SYSTEM; STORAGE; ROOT
  ; **NODE** ; EXPAND; QUEUE; ALLOCATE; NETWORK; **NODE** ; GENERATE; ROUTE;
  MESSAGE; BROADCAST
Index Terms/Additional Words: **PARA LLEL** ; IMPLEMENTATION; OF;
  COMBINATORIAL; OPTIMISATION
Derwent Class: T01
International Patent Class (Main): G06F-015/18
International Patent Class (Additional): **G06F-015/16**
File Segment: EPI

 14/5/22   (Item 22 from file: 351)
DIALOG(R)File 351:DERWENT WPI

010716457   **Image available**
WPI Acc No: 96-213412/199622
XRPX Acc No: N96-178842
    Parallel   processing **network - has pivot switches for performing
 communication between cluster of processors** matrix **sequence**

Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: DENNEAU M M; GRICE D G; HOCHSCHILD P H; STUNKEL C B
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week	
JP 8077128	A	19960322	JP 95179812	A	19950717	G06F-015/173	199622	B
US 5566342	A	19961015	US 94298828	A	19940831	G06F-013/00	199647	

Priority Applications (No Type Date): US 94298828 A 19940831
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
JP 8077128	A		8			
US 5566342	A		12			

Abstract (Basic): JP 8077128 A
      The network has several set pivot switches (34) connected to several **node** switch settings (30,32) respectively forming a cluster of processor. The cluster of processor **matrix** sequence and line are interconnected through a circuit. All pivot switches line are interconnected to the same line of the **node** switch settings.
      The communication between the cluster of processor are performed through the pivot switches. A circuit does not directly connects processing **nodes** (24,26).
      ADVANTAGE - Arranges large-scale connection between **processor array** **node** switch groups along with line and sequence by utilising switch setting added to processing **node** forming cluster of processor.
      Dwg.1/7
Title Terms: PARALLEL; PROCESS; NETWORK; PIVOT; SWITCH; **PERFORMANCE** ; COMMUNICATE; CLUSTER; PROCESSOR; **MATRIX** ; SEQUENCE
Derwent Class: T01
International Patent Class (Main): G06F-013/00; G06F-015/173
International Patent Class (Additional): **G06F-015/16**
File Segment: EPI

  14/5/23   **(Item 23 from file: 351)**
DIALOG(R)File 351:DERWENT WPI
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010474631   **Image available****
WPI Acc No: 95-375951/199549
  Node **coupling system for LAN, WAN - groups** node **based on dimensional co-ordinates, with secondary** nodes **mounted on substrate**
Patent Assignee: GIJUTSU KENKYUKUMIAI SHIN JOHO SHORI KAI (GIJU-N); TOSHIBA KK (TOKE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week	
JP 7200508	A	19950804	JP 93349337	A	19931228	G06F-015/173	199549	B

Priority Applications (No Type Date): JP 93349337 A 19931228
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
JP 7200508	A		18			

Abstract (Basic): JP 7200508 A
      The **node** coupling system has an element processor provided with n dimension mesh (00,01,02...) to form a link. A cross bar switch or a processor is connected to secondary **nodes** (S0-S3). The **nodes** are grouped based on the dimensional co-ordinates, to form n-1 meshes. The secondary **nodes** are mounted on a substrate.
      ADVANTAGE - Gives high mounting ease, number extendibility,

communication-link band width and random communication **performance** .
    Increases **matrix** multiplication efficiency and overall **performance** .
        Dwg.1/21
Title Terms: **NODE** ; COUPLE; SYSTEM; LAN; WAN; GROUP; **NODE** ; BASED;
  DIMENSION; CO; ORDINATE; SECONDARY; **NODE** ; MOUNT; SUBSTRATE
Derwent Class: T01; W01
International Patent Class (Main): G06F-015/173
International Patent Class (Additional): **G06F-015/16**
File Segment: EPI

  14/5/24   (Item 24 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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010276208   **Image available**
WPI Acc No: 95-177463/199523
Related WPI Acc No: 97-457115
XRPX Acc No: N95-139314
 Data flow microprocessor with vector operation function - has program
 unit assigning destination node **number to operands using data flow**
  graph **with stored operands given to operation unit**
Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP
  (MITQ)
Inventor: ASAI F; KOMORI S; TAKATA H; TAMURA T; TSUBOTA H
Number of Countries: 002 Number of Patents: 003
Patent Family:
Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
US 5404553	A	19950404	US 92819164	A	19920102	G06F-009/00	199523 B
JP 8212186	A	19960820	JP 91122338	A	19910424	G06F-015/82	199643
JP 2968060	B2	19991025	JP 9113959	A	19910109	G06F-009/46	199950

Priority Applications (No Type Date): JP 91122338 A 19910424; JP 9113959 A
    19910109; JP 9140981 A 19910212
Patent Details:
Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
US 5404553	A		110			
JP 8212186	A		57			
JP 2968060	B2		7	Previous Publ.		JP 4235636

Abstract (Basic): US 5404553 A
      The processor has an I/O interface unit transferring data with an
    operand to and from an external unit. A circuit generates a pair of the
    operands by detecting data packets with coincident destination **node**
    numbers. An operation unit receives the operands and produces a result
    depending on an attached instruction code and transfers the result to
    the I/O interface unit. A program memory unit operates on the operands
    by reading its stored data flow **graph** .
      The destination **node** number attached to the operands is addressed
    as an input address. The destination **node** number and tag information
    is updated using the data flow **graph** . The I/O interface unit, operand
    generating circuit, program memory unit and data memory are connected
    in a ring shape. When the instruction code attached to the data input
    to the data memory is a predetermined instruction, previously stored
    operands are given with the code to the operation unit and operated on
    in sequential order.
      ADVANTAGE - Provides complete control with small number of simple
    instructions. Capable of executing program at high efficiency while
    achieving high vector operation **performance** .
        Dwg.5/74
Title Terms: DATA; FLOW; MICROPROCESSOR; VECTOR; OPERATE; FUNCTION; PROGRAM
  ; UNIT; ASSIGN; DESTINATION; **NODE** ; NUMBER; OPERAND; DATA; FLOW; **GRAPH**

; STORAGE; OPERAND; OPERATE; UNIT
Derwent Class: T01
International Patent Class (Main): G06F-009/00; G06F-009/46; G06F-015/82
International Patent Class (Additional): G06F-009/38; G06F-017/16
File Segment: EPI

14/5/25   (Item 25 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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010130557   **Image available**
WPI Acc No: 95-031808/199505
Related WPI Acc No: 95-008225
XRPX Acc No: N95-025305
 Draw processor for high performance   3- D   graphics **accelerator -**
 performs scan edgewalking and scan interpolation functions to render 3-
  D **geometry object defined by draw packet**
Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: DEERING M F
Number of Countries: 004 Number of Patents: 003
Patent Family:
Patent No Kind Date   Applicat No Kind Date   Main IPC   Week
EP 631252 A2 19941228 EP 94302543 A   19940411 G06F-015/72   199505 B
US 5440682 A 19950808 US 9371699   A   19930604 G06F-015/00   199537
                       US 9382065   A   19930623
EP 631252 A3 19950315 EP 94302543 A   19940411 G06F-015/72   199542

Priority Applications (No Type Date): US 9382065 A 19930623; US 9371699 A
  19930604
Cited Patents: DE 3924759
Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
EP 631252   A2 E 29
   Designated States (Regional): DE GB NL
US 5440682 A   26 CIP of   US 9371699

Abstract (Basic): EP 631252 A
     The draw processor has a geometry pipeline interface circuit
  receiving a draw packet over a bus from a floating point processor. The
  draw packet contains a set of geometry parameters that define a
  geometry object including high level screen space descriptions of 2-D
  and **3 -D** point line and area **graphics** primitives. The interface
  adjusts the geometry parameters according to an interleave value
  corresp. to the draw processor. A rendering circuit receives the
  parameters and generates a pixel set corresp. to the object by
  performing edgewalking and scan interpolation functions according to
  the geometry parameters.
     A direct port interface receives a direct port packet over the draw
  bus from a command pre-processor. The direct port packet contains a set
  of pixel function parameters that control at least one pixel function
  of the draw processor. A memory control circuit receives the pixels and
  the pixel function parameters and writes the pixels into a frame memory
  buffer whilst performing the pixel function.
     USE/ADVANTAGE - Fast operation esp. for tessellated geometry. High
  rendering **performance** quality.
     Dwg.5/13
Title Terms: DRAW; PROCESSOR; HIGH; **PERFORMANCE** ; **GRAPHIC** ; ACCELERATE;
 PERFORMANCE ; SCAN; SCAN; INTERPOLATION; FUNCTION; RENDER; GEOMETRY;
  OBJECT; DEFINE; DRAW; PACKET
Derwent Class: T01
International Patent Class (Main): G06F-015/72

21 May 10, 2000 10:16

File Segment: EPI

 14/5/26   (Item 26 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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010106955   **Image available**
WPI Acc No: 95-008208/199502
XRPX Acc No: N95-006809
 Floating point processor for three- dimensional graphics **accelerator**
 - has specialised graphics **micro instruments for hardware re-mapping**
 general purpose registers to sort triangle vertices
Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: DEERING M F
Number of Countries: 005 Number of Patents: 004
Patent Family:
Patent No Kind Date   Applicat No Kind Date   Main IPC   Week
EP 627682 A1 19941207 EP 94302534 A 19940411 G06F-009/38   199502 B
US 5517611 A 19960514 US 9371709   A 19930604 G06F-015/16   199625
                        US 95506003 A 19950724
EP 627682 B1 19990526 EP 94302534 A 19940411 G06F-009/38   199925
DE 69418646 E 19990701 DE 618646   A 19940411 G06F-009/38   199932
                        EP 94302534 A 19940411

Priority Applications (No Type Date): US 9371709 A 19930604; US 95506003 A
   19950724
Cited Patents: EP 410778; GB 2186105; US 4107773; WO 8909447
Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
EP 627682   A1 E 33
   Designated States (Regional): DE FR GB NL
US 5517611 A   29 Cont of   US 9371709
EP 627682   B1 E
   Designated States (Regional): DE FR GB NL
DE 69418646 E   Based on   EP 627682

Abstract (Basic): EP 627682 A
      The floating-point processor for a high-**performance   three -
   dimensional graphics** accelerator in a computer system implements
   specialised **graphics** micro instructions. The specialised **graphics**
   micro-instructions include a swap micro instruction which causes a
   hardware re-mapping of general purpose register groups to sort
   triangle vertices . The **graphics** micro instructions also include
   specialised conditional branches for **three dimensional** geometry.
      The circuitry includes a multiple buffer input register file,
   multiple buffer output register file, and control sequencer for
   assembling the draw packet using floating-point compare and swap micro
   instructions. The swap micro instruction rearranges a register map for
   the first, second and third register groups.
      ADVANTAGE - Improves **graphics** accelerator **performance** while
   minimising costs.
      Dwg.3/16
Title Terms: FLOAT; POINT; PROCESSOR; **THREE -DIMENSIONAL ; GRAPHIC ;**
   ACCELERATE; SPECIAL; **GRAPHIC ;** MICRO; INSTRUMENT; HARDWARE; MAP; GENERAL
   ; PURPOSE; REGISTER; SORT; **TRIANGLE ; VERTEX**
Derwent Class: T01
International Patent Class (Main): G06F-009/38; **G06F-015/16**
International Patent Class (Additional): G06F-015/66; G06T-015/00
File Segment: EPI

14/5/27   (Item 27 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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010104922   **Image available**
WPI Acc No: 95-006175/199501
Related WPI Acc No: 90-044989
XRPX Acc No: N95-005127
Booting mode in distributed digital data processing system - performing boot retrieval operation in response to receipt by host of initiate boot image transfer request
Patent Assignee: DIGITAL EQUIP CORP (DIGI)
Inventor: CROLL J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
US 5367688	A	19941122	US 8793811	A	19870904	G06F-013/00	199501 B
			US 89384832	A	19890725		
			US 90555776	A	19900719		
			US 92827473	A	19920129		
			US 9333053	A	19930310		
			US 94229845	A	19940415 B		

Priority Applications (No Type Date): US 8793811 A 19870904; US 89384832 A
   19890725; US 90555776 A 19900719; US 92827473 A 19920129; US 9333053 A
   19930310; US 94229845 A 19940415
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
US 5367688	A		10	Div ex	US 8793811	
				Cont of	US 89384832	
				Cont of	US 90555776	
				Cont of	US 92827473	
				Cont of	US 9333053	
				Div ex		US 4885770

Abstract (Basic): US 5367688 A
      A distributed digital data processing system includes a host and at
   least one **node** interconnected by a communications link. In response
   to a boot command, the **node** requests its boot **image** from the host
   over the communications link. The host then provides pointers to
   portions of the boot **image** to the **node** . The **node** then retrieves
   the portions of the boot **image** identified by the pointers. These
   operations are repeated until **node** retrieves the entire boot **image** .
      By having the host supply pointers to the boot **image** and the
 node perform the retrieval operations in response to the pointers, the
   host is freed to perform other operations while the **node** is actually
   performing the retrieval operations.
      USE - Enabling booting of intelligent **node** connected to host
   system.
      Dwg.1/2
Title Terms: MODE; DISTRIBUTE; DIGITAL; DATA; PROCESS; SYSTEM; **PERFORMANCE**
 ; BOOT; RETRIEVAL; OPERATE; RESPOND; RECEIPT; HOST; INITIATE; BOOT;
 IMAGE ; TRANSFER; REQUEST
Derwent Class: T01
International Patent Class (Main): G06F-013/00
International Patent Class (Additional): **G06F-015/16**
File Segment: EPI

14/5/28   (Item 28 from file: 351)
DIALOG(R)File 351:DERWENT WPI
(c) 2000 Derwent Info Ltd. All rts. reserv.

009973545   **Image available**
WPI Acc No: 94-241258/199429
XRPX Acc No: N94-190224
 **Self-timed mesh routing chip with data broadcasting - passes message
 contg first and second data words from first processor** node **to first
 message routing device**
Patent Assignee: INTEL CORP (ITLC)
Inventor: DUNNING D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
US 5333279	A	19940726	US 92892535	A	19920601	G06F-013/14	199429 B

Priority Applications (No Type Date): US 92892535 A 19920601
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
US 5333279	A		18			

Abstract (Basic): US 5333279 A
       The appts providing for data broadcasting in a two dimensional mesh
    of processor **nodes** is disclosed. In accordance with the present
    invention, a self-timed message routing chip is coupled to each
    processor **node** , thereby forming a two dimensional mesh of message
    routing chips. Broadcasting originates from a **corner** node , and data
    can broadcast through the mesh routing chips to a row, a column, or a
    matrix of **nodes** .
       The mesh routing chips, together, form a self-timed pipeline with
    each individual message routing chip having broadcasting hardware which
    provides for the forking of a message within that particular message
    routing chip. The self-timed forking of a message within individual
    message routing chips directly supports data broadcasting within the
    two dimensional mesh.
       USE/ADVANTAGE - For routing and broadcasting data in
    two-dimensional mesh of processor **nodes** . Significant reduction of
    time required for broadcast task, hence improving **performance** of
    entire **parallel   processing** system
       Dwg.3/5
Title Terms: SELF; TIME; MESH; ROUTE; CHIP; DATA; BROADCAST; PASS; MESSAGE;
  CONTAIN; FIRST; SECOND; DATA; WORD; FIRST; PROCESSOR; **NODE** ; FIRST;
  MESSAGE; ROUTE; DEVICE
Derwent Class: T01
International Patent Class (Main): G06F-013/14
File Segment: EPI

 14/5/29   (Item 29 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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009934599   **Image available**
WPI Acc No: 94-202311/199425
XRPX Acc No: N94-159154
 **Parallel scalable internet working unit architecture - employs two
 network controllers, foreground and background buffer controller, both
 with local memory,** node **processor and buffer memory attached to IWU
 with individual PMI communicating with FGAM**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: YANG M S; YIH J
Number of Countries: 005 Number of Patents: 004
Patent Family:
Patent No Kind Date   Applicat No Kind Date   Main IPC   Week

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EP 604341   A2 19940629 EP 93480178  A  19931104 H04L-029/06   199425 B
JP 6237270  A  19940823 JP 93308196  A  19931208 H04L-012/56   199438
US 5465331  A  19951107 US 92996384  A  19921223 G06F-015/16   199550
EP 604341   A3 19960207 EP 93480178  A  19931104 H04L-029/06   199622
```

Priority Applications (No Type Date): US 92996384 A 19921223
Cited Patents: No-SR.Pub; 2.Jnl.Ref; EP 422910; EP 432346; FR 2603437
Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
EP 604341   A2 E 18
   Designated States (Regional): DE FR GB
JP 6237270 A   13
US 5465331 A   17

Abstract (Basic): EP 604341 A
     The system has a memory (112) for storing packets, and a background
   buffer controller coupled to the packet memory for organising and
   maintaining the packets in memory. A foreground buffer controller
   (FGAM) coupled between the foreground unit and the packet memory,
   transfers packets to and from the background unit (BGAM).
     Packets transferred from one of the networks to the packet memory,
   and from the packet memory to one of the networks pass through the
   foreground unit. A **node** processor (NP) is coupled to the foreground
   and background unit to access packets from the memory via the
   background unit.
     ADVANTAGE - Use of decentralisation of overall control of buffers
   by creating front end buffer controller allows for greater **parallel**
   processing of data transfer and control as well as greater
   scalability.
     Dwg.1/12
Title Terms: PARALLEL; WORK; UNIT; ARCHITECTURE; EMPLOY; TWO; NETWORK;
   CONTROL; FOREGROUND; BACKGROUND; BUFFER; CONTROL; LOCAL; MEMORY; **NODE** ;
   PROCESSOR; BUFFER; MEMORY; ATTACH; INDIVIDUAL; COMMUNICATE
Derwent Class: W01
International Patent Class (Main): **G06F-015/16** ; H04L-012/56; H04L-029/06
International Patent Class (Additional): G06F-013/00; H04J-003/02;
   H04L-012/66; H04L-013/08; H04L-013/10
File Segment: EPI

 14/5/30   (Item 30 from file: 351)
DIALOG(R)File 351:DERWENT WPI
(c) 2000 Derwent Info Ltd. All rts. reserv.

009866163   **Image available**
WPI Acc No: 94-146036/199418
XRPX Acc No: N94-115075
 Distributed data processing system - has several resources, **user**
 processes performing transactions accessing resources, resource
 manager responsive to lock requests transaction manager storing wait-for
  graph, **and cyclic chain od dependencies detector**
Patent Assignee: INT COMPUTERS LTD (INCM)
Inventor: VAN DEN BERG T W
Number of Countries: 006 Number of Patents: 007
Patent Family:
Patent No Kind Date   Applicat No Kind Date   Main IPC   Week
EP 595453   A1 19940504 EP 93306677 A 19930823 G06F-009/46   199418 B
AU 9349160 A 19940505 AU 9349160   A 19931022 G06F-015/16   199423
ZA 9306275 A 19940525 ZA 936275   A 19930826 G06F-000/00   199424
AU 662842   B 19950914 AU 9349160   A 19931022 G06F-015/16   199546
US 5459871 A 19951017 US 93112776 A 19930826 G06F-013/00   199547
EP 595453   B1 19981111 EP 93306677 A 19930823 G06F-009/46   199849
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DE 69322057 E   19981217 DE 622057    A  19930823 G06F-009/46    199905
                         EP 93306677  A  19930823
Priority Applications (No Type Date): GB 938877 A 19930429; GB 9222390 A
  19921024
Cited Patents: 04Jnl.Ref
Patent Details:
Patent    Kind Lan Pg Filing Notes      Application  Patent
EP 595453  A1 E  20
   Designated States (Regional): DE FR GB
ZA 9306275  A      43
AU 662842   B         Previous Publ.              AU 9349160
US 5459871  A      15
EP 595453   B1 E
   Designated States (Regional): DE FR GB
DE 69322057 E         Based on                    EP 595453

Abstract (Basic): EP 595453 A
        The distributed data processing system includes a distributed
   **resource**  manager which detects dependencies between transaction caused
   by conflicting lock request. A distributed transaction manager stores a
   wait-for **graph**  with **nodes**  representing transactions and edges the
   **nodes**  and represents dependencies between the transactions.
        Each edge is labelled with the identities of the lock requests that
   caused the dependency. The transaction manager propagates probes
   through the **graph**  to detect cyclic dependencies, indicating deadlock.
        ADVANTAGE - Improved deadlock detection and resolution.
        Dwg.1/4
Title Terms: DISTRIBUTE; DATA; PROCESS; SYSTEM; **RESOURCE** ; USER; PROCESS;
 **PERFORMANCE** ; TRANSACTION; ACCESS; **RESOURCE** ; **RESOURCE** ; MANAGE;
 RESPOND; LOCK; REQUEST; TRANSACTION; MANAGE; STORAGE; WAIT; **GRAPH** ;
 CYCLIC; CHAIN; OD; DETECT
Derwent Class: T01
International Patent Class (Main): G06F-000/00; G06F-009/46; G06F-013/00;
 **G06F-015/16**
International Patent Class (Additional): G06F-011/14; G06F-013/364
File Segment: EPI


 **14/5/31      (Item 31 from file: 351)**
DIALOG(R)File 351:DERWENT WPI
(c) 2000 Derwent Info Ltd. All rts. reserv.

009711707     **Image available**
WPI Acc No: 93-405260/199350
XRPX Acc No: N93-313728
 **Fault-tolerant mesh with spare**  nodes **in parallel or network**
 **architecture for massively parallel computer or other element array -**
 **adds spare components (** nodes) **and extra links (edges) to given target**
 **mesh of small degree so architecture can be reconfigured as operable**
 **target mesh in the presence of up to k faults, regardless of their**
 **distribution**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC  )
Inventor: BRUCK J; CYPHER R E; HO C
Number of Countries: 001  Number of Patents: 001
Patent Family:
Patent No  Kind  Date    Applicat No Kind  Date    Main IPC     Week
US 5271014  A   19931214 US 92878946  A   19920504 G06F-015/00   199350 B

Priority Applications (No Type Date): US 92878946 A 19920504
Patent Details:
Patent    Kind Lan Pg Filing Notes      Application  Patent
US 5271014  A      34

Abstract (Basic): US 5271014 A
        The network architecture tolerates up to k faults in a
    d-dimensional mesh architecture based on the approach of adding spare
    components (**nodes** ) and extra links (edges) to a given target mesh
    where m spare **nodes**   (mk) are added and the maximum number of links
    per **node**   (degree of the mesh) is kept small. The resulting
    architecture can be reconfigured, without the use of switches, as an
    operable target mesh in the presence of up to k faults, regardless of
    their distribution.
        Given a d-dimensional mesh architecture having N=n1multiplied
    byn2multiplied by. . . multiplied bynd **nodes** , the fault-tolerant mesh
    can be represented by a diagonal or circulant **graph**  having N+m-k
  **nodes** , where mk. This **graph**  has the property that given any set of k
    or fewer faulty **nodes** , the remaining **graph** , after the **performance**
    of a pre-determined **node**  renaming process, is guaranteed to contain
    as a subgraph the **graph**  corresponding to the target mesh M so long as
    d2 and nd3. The fault-tolerant mesh allows a healthy target mesh to be
    located in the presence of up to k faulty network components.
        USE/ADVANTAGE - Low redundancy cost handling of faults in mesh
    architectures, giving higher yield eg in WSI array mfr.
        Dwg.7/11
Title Terms: FAULT; TOLERATE; MESH; SPARE; **NODE** ; PARALLEL; NETWORK;
  ARCHITECTURE; PARALLEL; COMPUTER; ELEMENT; ARRAY; ADD; SPARE; COMPONENT;
 **NODE** ; EXTRA; LINK; EDGE; TARGET; MESH; DEGREE; SO; ARCHITECTURE; CAN;
  RECONFIGURE; OPERATE; TARGET; MESH; PRESENCE; UP; FAULT; DISTRIBUTE
Derwent Class: T01
International Patent Class (Main): G06F-015/00
File Segment: EPI


 **14/5/32     (Item 32 from file: 351)**
DIALOG(R)File 351:DERWENT WPI
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009491199    **Image available**
WPI Acc No: 93-184734/199323
Related WPI Acc No: 90-356929; 93-184732; 93-184733
XRPX Acc No: N93-141952
 **Re-configurable signal**  processor **performing**  concurrent **computations -
 realises generic capability for fault-tolerant and re-configurable
 multi-processor computer scalable to thousands of processor elements**
Patent Assignee: AMERICAN TELEPHONE & TELEGRAPH CO (AMTT  )
Inventor: GORIN A L; MAKOFSKY P A; MORTON N; OLIVER N C; SHIVELY R R;
  STANZIOLA C A
Number of Countries: 001  Number of Patents: 001
Patent Family:
Patent No  Kind  Date    Applicat No Kind  Date    Main IPC      Week
GB 2262175  A   19930609 GB 906712    A   19900326 G06F-011/20   199323 B
                         GB 931714    A   19930128 B

Priority Applications (No Type Date): US 89331411 A 19890331
Patent Details:
Patent   Kind Lan Pg Filing Notes     Application  Patent
GB 2262175  A      27 Derived from    GB 906712
Abstract (Basic): GB 2262175 A
        In the system controlled assembly of processing elements is
    interconnected as processing **nodes** . A desired topology of **nodes**  is
    embedded into a fixed lattice, comprising a remote command Host,
    multiple processor elements arrayed in one or more **matrices**  of **nodes**
    . Each element having multiple exterior ports accessing the processing
    capability of the element, and effecting signal routing within each
    processor element between its processing capability and any of the

multiple ports.
    For blocking signal routing at selected ports, selected ports of
the elements in each **matrix** are connected to selected ports of
neighbour elements, and for connecting selected ports of designated
elements either to selected element ports in a further **matrix** of
processor elements or to the Host. The Host conditions the element
ports to direct signals to and from only selected ones each element's
neighbouring processor elements, the conditioning means achieving a
desired interconnection topology for the **nodes** of the system.
    USE/ADVANTAGE - Enables or disables **nodes** as necessary by
revising communication paths. Adds steps to application program to
convey idealised or nominal system configuration.
    Dwg.8/16
Title Terms: CONFIGURATION; SIGNAL; PROCESSOR; **PERFORMANCE** ; CONCURRENT;
  COMPUTATION; REALISE; CAPABLE; FAULT; TOLERATE; CONFIGURATION; MULTI;
  PROCESSOR; COMPUTER; THOUSAND; PROCESSOR; ELEMENT
Derwent Class: T01
International Patent Class (Main): G06F-011/20
File Segment: EPI


 **14/5/33      (Item 33 from file: 351)**
DIALOG(R)File 351:DERWENT WPI
(c) 2000 Derwent Info Ltd. All rts. reserv.

009335295     **Image available**
WPI Acc No: 93-028758/199304
XRPX Acc No: N93-021984
 **Multiprocessor scientific** visualisation **system - includes number of**
 **processor** nodes, **each including data processor which generates buffers**
 **byte enable signals and control signals**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC  )
Inventor: FOSTER D J; GARCIA A; PEARSON R B; CARCIA A
Number of Countries: 006  Number of Patents: 003
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Main IPC | Week | |
|---|---|---|---|---|---|---|---|---|
| EP 524683 | A1 | 19930127 | EP 92202126 | A | 19920711 | G06F-013/40 | 199304 | B |
| CA 2068580 | A | 19930123 | CA 2068580 | A | 19920513 | G06F-015/16 | 199314 | |
| US 5327570 | A | 19940705 | US 91734432 | A | 19910722 | G06F-009/00 | 199426 | |

Priority Applications (No Type Date): US 91734432 A 19910722
Cited Patents: EP 369265; EP 379768
Patent Details:

| Patent | Kind | Lan | Pg | Filing Notes | Application | Patent |
|---|---|---|---|---|---|---|
| EP 524683 | A1 | E | 75 | | | |

    Designated States (Regional): DE FR GB IT

| US 5327570 | A | | 51 |
|---|---|---|---|

Abstract (Basic): EP 524683 A
    The system comprises a number of processor **nodes** each including a
data processor (22a,28a) and a device, coupled to each of the **nodes** ,
for buffering data written by the associated data processor to a first
bus (23c), prior to the data being transmitted to a second bus (32). A
device, coupled to each of the **nodes** , buffers byte enable signals
generated by the associated data processor in conjunction with the data
written by the data processor. A device transmits the buffered data to
the second bus, the transmitting device including a device responsive
to the stored byte enable signals, for also transmitting a control
signal to the second bus for indicating if a memory write operation is
to be accomplished as a read-modify-write type of operation.
    A device couples the data, the control signal, and the byte enable
signals from the second bus to a third bus (24) for reception to a

memory shared by all of the data processors.
        USE/ADVANTAGE - High **performance** multiprocessor system.
    Efficiently utilises shared **resources** .
        m
        Dwg.2/26
Title Terms: MULTIPROCESSOR; SCIENCE; **VISUAL** ; SYSTEM; NUMBER; PROCESSOR;
  **NODE** ; DATA; PROCESSOR; GENERATE; BUFFER; BYTE; ENABLE; SIGNAL; CONTROL;
  SIGNAL
Derwent Class: T01
International Patent Class (Main): G06F-009/00; G06F-013/40; **G06F-015/16**
International Patent Class (Additional): G06F-013/36
File Segment: EPI


 **14/5/34      (Item 34 from file: 351)**
DIALOG(R)File 351:DERWENT WPI
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009166154     **Image available**
WPI Acc No: 92-293588/199236
Related WPI Acc No: 90-211351
XRPX Acc No: N92-224921
 **Centralised and distributed wait depth limited** concurrency **control –
 taking into account progress made by translations in conflict resolution
 in restarting translations by taking account of wait depth tree compared
 with predetermined value**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC  )
Inventor: FRANASZEK P A; ROBINSON J T; THOMASIAN A
Number of Countries: 004  Number of Patents: 003
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Main IPC | Week | |
|---|---|---|---|---|---|---|---|---|
| EP 501025 | A2 | 19920902 | EP 91121110 | A | 19911209 | G06F-015/403 | 199236 | B |
| US 5193188 | A | 19930309 | US 89294334 | A | 19890105 | G06F-015/40 | 199312 | |
| | | | US 91660762 | A | 19910225 | | | |
| EP 501025 | A3 | 19921230 | EP 91121110 | A | 19911209 | G06F-015/403 | 199345 | |

Priority Applications (No Type Date): US 91660762 A 19910225; US 89294334 A
  19890105
Cited Patents: No-SR.Pub; 2.Jnl.Ref
Patent Details:

| Patent | Kind | Lan | Pg | Filing Notes | Application | Patent |
|---|---|---|---|---|---|---|
| EP 501025 | A2 | E | 19 | | | |

    Designated States (Regional): DE FR GB

| US 5193188 | A | | 18 | CIP of | US 89294334 | |

Abstract (Basic): EP 501025 A
        A wait depth data structure is maintained which **graphically**
    describes a waiting depth of transactions being processed by the system
    where, for each transaction, a real-valued function provides a measure
    of current length lof a transaction.
        For each request for a lock, the wait depth data structure is
    tested for exceeding a predetermined value. The real-valued function is
    used to determine and restart the subset of transactions in the case of
    conflict between transactions so that the wait depth is reduced or kept
    below a predetermined value.
        USE/ADVANTAGE - **Concurrency** control in multi-user data
    processing environment. Minimises unnecessary lock conflicts. Restricts
    depth of waiting tree. Avoids **throughput** limitation and deadlock
    detection problems under conditions of high data contention.
        Dwg.1/9
Title Terms: CENTRE; DISTRIBUTE; WAIT; DEPTH; LIMIT; CONTROL; ACCOUNT;
  PROGRESS; MADE; TRANSLATION; CONFLICT; RESOLUTION; RESTART; TRANSLATION;

ACCOUNT; WAIT; DEPTH; TREE; COMPARE; PREDETERMINED; VALUE
Derwent Class: T01
International Patent Class (Main): G06F-015/40; G06F-015/403
File Segment: EPI


 **14/5/35      (Item 35 from file: 351)**
DIALOG(R)File 351:DERWENT WPI
(c) 2000 Derwent Info Ltd. All rts. reserv.

009074435     **Image available**
WPI Acc No: 92-201854/199225
XRPX Acc No: N92-152755
 **Computer system**  graphically **configuring data processing network - using
 ions to enable users to define multiple network**  nodes,  resources
 **associated with them and connections between them**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC  ); IBM CORP (IBMC  )
Inventor: MARTIN J S; SANCHEZ-FRANK A; SIRKIN M J
Number of Countries: 005  Number of Patents: 007
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Main IPC | Week | |
|---|---|---|---|---|---|---|---|---|
| EP 490624 | A2 | 19920617 | EP 91311452 | A | 19911210 | G06F-015/16 | 199225 | B |
| US 36444 | E | 19991214 | US 90625249 | A | 19901210 | G06F-003/00 | 200005 | |
| | | | US 93120313 | A | 19930913 | | | |
| | | | US 97806227 | A | 19970224 | | | |
| JP 4260149 | A | 19920916 | JP 91267127 | A | 19910918 | G06F-013/00 | 199244 | |
| US 5394522 | A | 19950228 | US 90625249 | A | 19901210 | G06F-015/62 | 199514 | |
| | | | US 93120313 | A | 19930913 | | | |
| EP 490624 | A3 | 19940119 | EP 91311452 | A | 19911210 | G06F-015/16 | 199517 | |
| EP 490624 | B1 | 19990414 | EP 91311452 | A | 19911210 | G06F-015/16 | 199919 | |
| DE 69131122 | E | 19990520 | DE 631122 | A | 19911210 | G06F-015/16 | 199926 | |
| | | | EP 91311452 | A | 19911210 | | | |


Priority Applications (No Type Date): US 90625249 A 19901210; US 93120313 A
   19930913; US 97806227 A 19970224
Cited Patents: -SR.Pub; 2.Jnl.Ref;  US 4813013
Patent Details:

| Patent | Kind | Lan | Pg | Filing Notes | Application | Patent |
|---|---|---|---|---|---|---|
| EP 490624 | A2 | E | 18 | | | |
| Designated States | | | | (Regional): DE FR GB | | |
| US 36444 | E | | | Cont of | US 90625249 | |
| | | | | Reissue of | | US 5394522 |
| JP 4260149 | A | | 12 | | | |
| US 5394522 | A | | 17 | Cont of | US 90625249 | |
| EP 490624 | B1 | E | | | | |
| Designated States | | | | (Regional): DE FR GB | | |
| DE 69131122 | E | | | Based on | | EP 490624 |


Abstract (Basic): EP 490624 A
        The computer system **graphically**  represents a network of three or
    more **nodes**  by defining network objects for the **nodes** , and
    **graphically**  defines connections to relate the network objects. The
    system also automatically generates parameters to configure a physical
    network as defined by the network objects and connections.
        Preferably, the user defines multiple network work station **nodes**
    using icons (13), specifies the **resources**  associate with each icon
    (12), and defined connections between icons using specified protocol
    constraints. The computer validates the network so defined and
    generates the associated configuration files for the respective work
    station **nodes** . The configuration files for the respective work
    stations in the network are preferably distributed and installed using
    the network **resources** . The network topology information so created

can be stored, retrieved and modified as necessary.
        ADVANTAGE - Meets needs of evolving network
Title Terms: COMPUTER; SYSTEM; **GRAPHICAL** ; DATA; PROCESS; NETWORK; ION;
  ENABLE; USER; DEFINE; MULTIPLE; NETWORK; **NODE** ; **RESOURCE** ; ASSOCIATE;
  CONNECT
Derwent Class: T01
International Patent Class (Main): G06F-003/00; G06F-013/00; **G06F-015/16** ;
  G06F-015/62
International Patent Class (Additional): G06F-015/00; H04L-012/24;
  H04L-012/26
File Segment: EPI


 **14/5/36      (Item 36 from file: 351)**
DIALOG(R)File 351:DERWENT WPI
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009056470    **Image available**
WPI Acc No: 92-183861/199222
XRPX Acc No: N92-138707
 **Computational model for dynamically configured systems - has various
 processing components created dynamically interfaced to each other and
 scheduled upon demand**
Patent Assignee: UNIV VANDERBILT (UYVA-N)
Inventor: BIEGL C; KARSAI G; SZTIPANOVITS J
Number of Countries: 017   Number of Patents: 003
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Main IPC | Week | |
|-----------|------|------|-------------|------|------|----------|------|---|
| WO 9208196 | A1 | 19920514 | WO 91US7397 | A | 19911007 | G06F-013/14 | 199222 | B |
| AU 9188457 | A | 19920526 | AU 9188457 | A | 19911007 | G06F-013/14 | 199235 | |
| | | | WO 91US7397 | A | 19911007 | | | |
| US 5249274 | A | 19930928 | US 90602961 | A | 19901024 | G06F-015/16 | 199340 | |

Priority Applications (No Type Date): US 90602961 A 19901024
Cited Patents: US 4447875; US 4849905; US 4922413
Patent Details:

| Patent | Kind | Lan | Pg | Filing Notes | Application | Patent |
|--------|------|-----|-----|-------------|-------------|--------|
| WO 9208196 | A1 | E | 24 | | | |

    Designated States (National): AU CA JP
    Designated States (Regional): AT BE CH DE DK ES FR GB GR IT LU NL SE

| AU 9188457 | A | | | Based on | WO 9208196 | |
| US 5249274 | A | | 13 | | | |

Abstract (Basic): WO 9208196 A
    A knowledge-based interpreter generates executable code to
    represent the engineering application of the scheduling and apparatus
    for model-based dynamically configured systems. The interpreter
    configures the final system from elementary building blocks such as
    signal processing routines or controller modules. The system
    configuration is generated dynamically from the model. The model and
    the system can be modified during system operation to relect changes in
    the environment.
    The central structure of the system is represented by models or
    **graphs** which are built up of actor **nodes** , data **nodes** and
    connection specifications. Each actor **node** is associated with a
    particular computational unit and with a local data structure. The
    actor **nodes** perform transformations on data streams by running an
    application module. Data **nodes** store either raw data, data produced
    by actor **nodes** or point to data.
    A cross correlator takes samples (10, 12) and performs fast
    Fourier transforms (14) and squares (16). An inverse fast Fourier
    transform (18) is averaged (20,22) and the result displayed (24).

ADVANTAGE - Improved **performance** of data driven and demand
driven.
  Dwg.1/6
Title Terms: COMPUTATION; MODEL; DYNAMIC; CONFIGURATION; SYSTEM; VARIOUS;
 PROCESS; COMPONENT; DYNAMIC; INTERFACE; SCHEDULE; DEMAND
Derwent Class: T01
International Patent Class (Main): G06F-013/14; **G06F-015/16**
File Segment: EPI


 **14/5/37**  **(Item 37 from file: 351)**
DIALOG(R)File 351:DERWENT WPI
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008866596  **Image available**
WPI Acc No: 91-370622/199151
XRPX Acc No: N91-283748
 **Symmetric linear system solving device using super-computer - perform**
 vector processing **at high-speed with reduced memory requirement over**
 **conventional scalar method**
Patent Assignee: NEC CORP (NIDE )
Inventor: HAYAMI K; WATANABE H
Number of Countries: 006 Number of Patents: 005
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Main IPC | Week | |
|-----------|------|------|-------------|------|------|----------|------|---|
| EP 461608 | A | 19911218 | EP 91109544 | A | 19910611 | | 199151 | B |
| CA 2044313 | A | 19911213 | | | | | 199210 | |
| US 5200915 | A | 19930406 | US 91712890 | A | 19910612 | G06F-007/38 | 199316 | |
| CA 2044313 | C | 19940322 | CA 2044313 | A | 19910611 | G06F-007/38 | 199417 | |
| EP 461608 | A3 | 19940518 | EP 91109544 | A | 19910611 | | 199524 | |

Priority Applications (No Type Date): JP 90151664 A 19900612
Cited Patents: NoSR.Pub; 6.Jnl.Ref
Patent Details:

| Patent | Kind | Lan | Pg | Filing Notes | Application | Patent |
|--------|------|-----|----|----|----|----|
| EP 461608 | A | | | | | |

 Designated States (Regional): DE FR GB

| US 5200915 | A | | 14 | | | |

Abstract (Basic): EP 461608 A
  The device solves a symmetric linear system, typically represented
by the **matrices** Au=b, where it is necessary for input data to prepare
only a right hand side vector of an equation, a diagonal **matrix** and
either an upper or lower **triangular** **matrix** .
  The device is supplied with the two-dimensional arrays AA and JA,
and the one-dimensional array B. Following pointer array construction
and **matrix** decomposition, iteration in conjunction with first and
second product vectors yields the solution vector.
  u.
  ADVANTAGE - Requires less memory in supercomputer than
conventional calculation method, by utilising high-speed **vector**
 **processing** technique. (12pp Dwg.No.2/6)
Title Terms: SYMMETRICAL; LINEAR; SYSTEM; SOLVING; DEVICE; SUPER; COMPUTER;
 **PERFORMANCE** ; VECTOR; PROCESS; HIGH; SPEED; REDUCE; MEMORY; REQUIRE;
 CONVENTION; SCALE; METHOD
Derwent Class: T01
International Patent Class (Main): G06F-007/38
International Patent Class (Additional): G06F-015/34
File Segment: EPI


 **14/5/38**  **(Item 38 from file: 351)**

DIALOG(R)File 351:DERWENT WPI
(c) 2000 Derwent Info Ltd. All rts. reserv.

008661387     **Image available**
WPI Acc No: 91-165414/199123
XRPX Acc No: N91-126838
 **Multiprocessor with crossbar between processors and memories –
 establishes processor memory links individual processors switch and
 memories on single silicon chip**
Patent Assignee: TEXAS INSTR INC (TEXI   )
Inventor: GOVE R J; GUTTAG K M; INSIMMONS N K; BALMER K; ING-SIMMONS N K
Number of Countries: 007   Number of Patents: 009
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Main IPC | Week | |
|---|---|---|---|---|---|---|---|---|
| EP 429733 | A | 19910605 | EP 89313252 | A | 19891219 | | 199123 | B |
| JP 3026984 | B2 | 20000327 | JP 89338040 | A | 19891226 | G06F-015/173 | 200020 | |
| EP 429733 | A3 | 19930303 | EP 89313252 | A | 19891219 | | 199349 | |
| US 5471592 | A | 19951128 | US 89435591 | A | 19891117 | G06F-013/00 | 199602 | |
| | | | US 92933865 | A | 19920821 | | | |
| | | | US 93135754 | A | 19931012 | | | |
| | | | US 94263504 | A | 19940621 | | | |
| US 5592405 | A | 19970107 | US 89435591 | A | 19891117 | G06F-007/38 | 199708 | |
| | | | US 92933865 | A | 19920821 | | | |
| | | | US 93135754 | A | 19931012 | | | |
| | | | US 94263504 | A | 19940621 | | | |
| | | | US 95484579 | A | 19950607 | | | |
| US 5606520 | A | 19970225 | US 89435591 | A | 19891117 | G06F-007/38 | 199714 | |
| | | | US 92933865 | A | 19920821 | | | |
| | | | US 93135754 | A | 19931012 | | | |
| | | | US 94263504 | A | 19940621 | | | |
| | | | US 95484540 | A | 19950607 | | | |
| US 5696913 | A | 19971209 | US 89435591 | A | 19891117 | G06F-013/00 | 199804 | |
| | | | US 92933865 | A | 19920821 | | | |
| | | | US 93135754 | A | 19931012 | | | |
| | | | US 94263504 | A | 19940621 | | | |
| | | | US 95472827 | A | 19950607 | | | |
| EP 429733 | B1 | 19990428 | EP 89313252 | A | 19891219 | G06F-015/16 | 199921 | |
| DE 68928980 | E | 19990602 | DE 628980 | A | 19891219 | G06F-015/16 | 199928 | |
| | | | EP 89313252 | A | 19891219 | | | |

Priority Applications (No Type Date): US 89435591 A 19891117; US 92933865 A
   19920821; US 93135754 A 19931012; US 94263504 A 19940621; US 95484579 A
   19950607; US 95484540 A 19950607; US 95472827 A 19950607
Cited Patents: NoSR.Pub; 1.Jnl.Ref; EP 245996; US 4633245; WO 8808167
Patent Details:

| Patent | Kind | Lan | Pg | Filing Notes | Application | Patent |
|---|---|---|---|---|---|---|
| EP 429733 | A | | 153 | | | |
| Designated States (Regional): DE FR GB IT NL | | | | | | |
| JP 3026984 | B2 | | 85 | Previous Publ. | | JP 3211656 |
| EP 429733 | A3 | | 153 | | | |
| US 5471592 | A | | 69 | Cont of | US 89435591 | |
| | | | | Cont of | US 92933865 | |
| | | | | Cont of | US 93135754 | |
| US 5592405 | A | | 71 | Cont of | US 89435591 | |
| | | | | Cont of | US 92933865 | |
| | | | | Cont of | US 93135754 | |
| | | | | Div ex | US 94263504 | |
| | | | | Div ex | | US 5471592 |
| US 5606520 | A | | 101 | Cont of | US 89435591 | |
| | | | | Cont of | US 92933865 | |
| | | | | Cont of | US 93135754 | |
| | | | | Div ex | US 94263504 | |

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                       Div ex                       US 5471592
US 5696913  A    140 Cont of        US 89435591
                       Cont of        US 92933865
                       Cont of        US 93135754
                       Div ex         US 94263504
                       Div ex                       US 5471592
EP 429733   B1 E
    Designated States (Regional): DE FR GB IT NL
DE 68928980 E          Based on                     EP 429733
```

Abstract (Basic): EP 429733 A
     The multi-processing system has n processors, each operable from
  instruction sets provided from a memory source for controlling a number
  of different processes, said processes relying on the movement of data
  to or from one or more addressable memories. Memory sources, each have
  a unique addressable space. M is greater than n. A switch **matrix** is
  connected to the memories and is connected to the processors. The
  switch **matrix** is enabled on a processor cycle by cycle basis for
  interconnecting any of the processors with any of the memories for the
  interchange between the memories and the connected processors of
  instruction sets from one or more addressable memory spaces and data
  from other addressable memory spaces.
     A common instruction set is capable of operating w.r.t. each other
  in a **parallel processing capacity** from the same or different
  instruction streams from the common instruction set and one other
  processor operable with a different instruction set.
     ADVANTAGE - High operational flexibility. (153pp Dwg.No.1/61
Title Terms: MULTIPROCESSOR; CROSSBAR; PROCESSOR; MEMORY; ESTABLISH;
  PROCESSOR; MEMORY; LINK; INDIVIDUAL; PROCESSOR; SWITCH; MEMORY; SINGLE;
  SILICON; CHIP
Derwent Class: T01
International Patent Class (Main): G06F-007/38; G06F-013/00; **G06F-015/16** ;
  G06F-015/173
International Patent Class (Additional): G06F-007/00; G06F-007/50;
  G06F-012/00; G06F-012/06
File Segment: EPI

 14/5/39   (Item 39 from file: 351)
DIALOG(R)File 351:DERWENT WPI
(c) 2000 Derwent Info Ltd. All rts. reserv.

008646277   **Image available**
WPI Acc No: 91-150306/199121
XRPX Acc No: N91-115416
    Processor   array **system with an SIMD architecture - has sub-array
 modules, each module having 32 processing elements, byte-wide arithmetic
 unit and multi-byte shift network**
Patent Assignee: AMT HOLDINGS LTD (AMTH-N)
Inventor: HUNT D
Number of Countries: 013 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
EP 428327	A	19910522	EP 90312204	A	19901108		199121 B

Priority Applications (No Type Date): GB 8925721 A 19891114
Cited Patents: EP 191280; US 4144566
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
EP 428327	A					

    Designated States (Regional): AT BE CH DE ES FR GB GR IT LI LU NL SE

Abstract (Basic): EP 428327 A
     The **processor   array** system employing an SIMD architectures
comprises a number of sub-arrays (S1...S4) modules. Each sub-array
includes n=32 processing elements (PE). Each processing element is
connected to a local store comprising on-chip memory; each chip is
connected by an m-bit wide path (where m is greater than 1) to a block
region of off-chip memory. The m-bit wide path is selectively
configurable as one bit path to or from each of m processor elements,
or as an m-bit wide path arranged to communicate complete m-bit words
of memory data between the region of off-chip memory and respective
processing elements.
     Each processing element includes a byte-wide arithmetic unit (ALU)
and byte-wide data paths for carrying data between the ALU and the on
chip memory; each processing element further includes a four byte wide
32 bit operand shift network (Q) comprising a byte-wise shift network
(Q1), and a bit-wise shift network (Q2) and an output register (Q0).
Such **processor   array** system is pref. connected to a host processor
arranged to address the array as an extension of its own memory, via a
scalar processor interface (MCU) for controlling the operation of the
array.
     USE/ADVANTAGE - **Parallel processing** computer systems, scan
array system with SIMD architecture; significant improvement in
performance of system when handling **matrices** , and **corner** turning
can be carried out in transit between off-chip memory and the
processing element using an n bit shift register, and arranging the
off-chip memory in horizontal mode with a word length equal to number
of processing elements. (Dwg.No.1/5)
Title Terms: PROCESSOR; ARRAY; SYSTEM; SIMD; ARCHITECTURE; SUB; ARRAY;
  MODULE; MODULE; PROCESS; ELEMENT; ARITHMETIC; UNIT; MULTI; BYTE; SHIFT;
  NETWORK
Derwent Class: T01
International Patent Class (Additional): G06F-015/80
File Segment: EPI

 14/5/40   (Item 40 from file: 351)
DIALOG(R)File 351:DERWENT WPI
(c) 2000 Derwent Info Ltd. All rts. reserv.

008622624   **Image available**
WPI Acc No: 91-126654/199118
XRPX Acc No: N91-097467
   Graphics **display system parametric curve evaluation method - stores
 NURBS data as sequence of records used to evaluate coordinates of
 determined parameter points along the curve**
Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: LUKEN W L
Number of Countries: 005 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week	
EP 425174	A	19910502	EP 90311369	A	19901017		199118	B
EP 425174	A3	19921007	EP 90311369	A	19901017		199340	
US 5317682	A	19940531	US 89426912	A	19891024	G06F-015/62	199421	
			US 92821246	A	19920110			
			US 936713	A	19930121			

Priority Applications (No Type Date): US 89426912 A 19891024; US 92821246 A
  19920110; US 936713 A 19930121
Cited Patents: NoSR.Pub; 1.Jnl.Ref; EP 277832; EP 314335; US 4760548
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
EP 425174	A					

Designated States (Regional): DE FR GB IT
US 5317682 A   23 Cont of   US 89426912
                      Cont of   US 92821246

Abstract (Basic): EP 425174 A
       The method of converting NURBS data representative of parametric
    curve into geometric coordinates of **vertices** of a polyline for
    subsequent display, the curve being composed of successive spans,
    involves organizing and locating the data in memory as a sequence of
    data records. A first subset of the sequence defines a first span of
    the curve with each successive record defining a corresponding span.
       The first set of data records are read and used to evaluate the
    coordinates of determined parameter points along the first span of the
    curve, with successive points evaluated form successive records.
       USE/ADVANTAGE - Evaluating and rendering curves for computer
  graphics display system offers high **performance** , good numerical
    stability, cost effectiveness, high speed and accuracy and has the
    advantages of NURBS. (26pp Dwg.No.4/11F)
Title Terms: **GRAPHIC** ; DISPLAY; SYSTEM; PARAMETER; CURVE; EVALUATE; METHOD
  ; STORAGE; DATA; SEQUENCE; RECORD; EVALUATE; COORDINATE; DETERMINE;
    PARAMETER; POINT; CURVE
Derwent Class: T01
International Patent Class (Main): G06F-015/62
International Patent Class (Additional): G06F-015/35
File Segment: EPI

 14/5/41   (Item 41 from file: 351)
DIALOG(R)File 351:DERWENT WPI
(c) 2000 Derwent Info Ltd. All rts. reserv.

008540862   **Image available**
WPI Acc No: 91-044925/199107
XRPX Acc No: N91-034966
 Multiprocessor system for graphic **data processing - performs display
 processing in all processors using associated** image **memory regions**
Patent Assignee: FRAUNHOFER-GES FORD ANGE (FRAU); FRAUNHOFER GES
   FOERDERUNG (FRAU)
Inventor: HAAKER T; JOSEPH H; SELZER H
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week	
DE 3924759	A	19910207	DE 3924759	A	19890726		199107	B
DE 3924759	C	19921015	DE 3924759	A	19890726	G06F-015/66	199242	

Priority Applications (No Type Date): DE 3924759 A 19890726
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
DE 3924759	C		9			

Abstract (Basic): DE 3924759 A
       A multiprocessor system for **graphical** processing performs
    geometric processing of geometric objects in several processors and
    forms **image** point data values in an output region from transformed
    coordinate values. The data values are placed in an **image** memory.
       The processors perform the display processing whereby all
  processors   simultaneously contain the results of the geometric
    object for **image** processing and the **image** point data associated
    with each processor are placed in an associated memory region.
       ADVANTAGE - The multiprocessor system eliminates data sensitivity
    and dynamically allocates processing power to ensure no processing
  capacity is wasted. (9pp Dwg.No.5/5)

Title Terms: MULTIPROCESSOR; SYSTEM; **GRAPHIC** ; DATA; PROCESS; **PERFORMANCE**
  ; DISPLAY; PROCESS; PROCESSOR; ASSOCIATE; **IMAGE** ; MEMORY; REGION
Derwent Class: T01
International Patent Class (Main): G06F-015/66
International Patent Class (Additional): **G06F-015/16**
File Segment: EPI

 14/5/42   (Item 42 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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008503307   **Image available**
WPI Acc No: 91-007391/199101
XRPX Acc No: N91-005792
 Single layer parallel **distributed** processing **network - has number of**
  nodes **with inputs and outputs connected to head to tail forming weighted**
  circuit defined by matrix
Patent Assignee: DU PONT DE NEMOURS & CO E I (DUPO); SAMARDZIJA N
  (SAMA-I)
Inventor: SAMARDZIJA N
Number of Countries: 015 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week	
WO 9015390	A	19901213					199101	B
CA 2017835	A	19901202					199109	
EP 474747	A	19920318	EP 90909020	A	19900521		199212	
JP 4505678	W	19921001	JP 90508502	A	19900521	G06G-007/60	199246	
			WO 90US2699	A	19900521			
EP 474747	A4	19930602	EP 90909020	A	19900000		199526	

Priority Applications (No Type Date): US 89360804 A 19890602
Cited Patents: US 4731747; US 4752906; US 4809193; 2.Jnl.Ref
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
WO 9015390	A					

    Designated States (National): JP
    Designated States (Regional): AT BE CH DE DK ES FR GB IT LU NL SE
EP 474747   A   48
    Designated States (Regional): AT BE CH DE DK ES FR GB IT LI LU NL SE
JP 4505678 W   17 Based on   WO 9015390

Abstract (Basic): WO 9015390 A
      The network (10) consists of a **matrix** of N **nodes** in the form of
  amplifiers (12) which represent an N by N information storage **matrix** ,
  A. The output port of each amplifier (20) is connected to a circuit
  which performs synaptic squashing (26). The output of the squasher (26)
  is connected to either the inverting port (16) or noninverting port
  (18) of some or all of the amplifiers (12) in the network (10)
  according to the sign of the value of the corresp. element in the
  matrix , A. The absolute value of the element set by each connectivity
  resistor (34).
      A similarity transformation **matrix** , T, is an N by N **matrix**
  whose columns are formed from a number of system output vectors and
  arbitrary vectors. The **matrix** product of A and T must equal the
  matrix product of T and a **matrix** of the eigenvalues of A.
      ADVANTAGE - Improves computation **performance** . (48pp Dwg.No.1/)
Title Terms: SINGLE; LAYER; PARALLEL; DISTRIBUTE; PROCESS; NETWORK; NUMBER;
  NODE ; INPUT; OUTPUT; CONNECT; HEAD; TAIL; FORMING; WEIGHT; CIRCUIT;
  DEFINE; **MATRIX**
Derwent Class: T01; T02
International Patent Class (Main): G06G-007/60

International Patent Class (Additional): G06F-013/00; G06F-015/18
File Segment: EPI

14/5/43   (Item 43 from file: 351)
DIALOG(R)File 351:DERWENT WPI
(c) 2000 Derwent Info Ltd. All rts. reserv.

008469929   **Image available**
WPI Acc No: 90-356929/199048
XRPX Acc No: N90-272585
 Embedding desired node **interconnection in processor - using tree
 expansion scheme to upsize processing element count, and selecting parent
 and child units**
Patent Assignee: AMERICAN TELEPHONE & TELEGRAPH CO (AMTT)
Inventor: GORIN A L; MAKOFSKY P A; MORTON N; OLIVER N C; SHIVELY R R;
  STANZIOLA C A
Number of Countries: 003 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week	
GB 2231985	A	19901128	GB 9067125	A	19900326		199048	B
CA 2008902	A	19900930					199051	
US 5020059	A	19910528	US 89331411	A	19890331		199124	
GB 2231985	B	19931215	GB 906712	A	19900326	G06F-011/20	199350	
CA 2008902	C	19940531	CA 2008902	A	19900130	G06F-015/16	199427	

Priority Applications (No Type Date): US 89331411 A 19890331
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
GB 2231985	B		2			

Abstract (Basic): GB 2231985 A
     The process for embedding a desired **node** interconnection topology
  in an assembly of processing elements fixedly interconnected through
  controllably enabled element ports, involves defining a desired
  operating processor element interconnection topology. A processor
  element port-to-port arrangement for the given assembly is determined
  which maximises processor element usage. The processor element **node**
  topology is embedded into the assembly by enabling selected element
  ports. A desired tree **node** topology is embedded in an assembly of
  processing elements by defining a desired tree **node** interconnection
  topology.
     A processor element port-to-port connection arrangement is
  determined for the given assembly which maximises use of processors
  known to be operable. The port-to-port connection arrangement is
  modified to minimise tree depth and the modified processor element
  connection arrangement is embedded into the assembly of elements by
  enabling selected processor element ports. The run **performance** of the
  operating processor element is monitored to detect elements which
  become inoperable. The port-to-port connection arrangements are
  modified to minimise tree depth and to make maximum use of remaining
  operable processor elements.
     ADVANTAGE - Improved fault tolerance. Reconfigurable. (45pp
  Dwg.No.5/16
Title Terms: EMBED; **NODE** ; INTERCONNECT; PROCESSOR; TREE; EXPAND; SCHEME;
  PROCESS; ELEMENT; COUNT; SELECT; PARENT; CHILD; UNIT
Derwent Class: T01; T04
International Patent Class (Main): G06F-011/20; **G06F-015/16**
File Segment: EPI

                                                                    .

 14/5/44   (Item 44 from file: 351)

DIALOG(R)File 351:DERWENT WPI
(c) 2000 Derwent Info Ltd. All rts. reserv.

008404774   **Image available**
WPI Acc No: 90-291775/199039
XRPX Acc No: N90-224630
 **Parallel structure for modelling and training neutral networks - gives
 significantly effective** performance **in unsupervised learning
 environments**
Patent Assignee: BODENSEEWERK GERAETETECH GMBH (PEKE); BODENSEEW
  GERATETEC (PEKE)
Inventor: HAEUSING M; HESSE H K; HESSE H
Number of Countries: 005 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
EP 388806	A	19900926	EP 90104969	A	19900316		199039 B
DE 3909153	A	19900927	DE 3909153	A	19890321		199040
EP 388806	A3	19920102	EP 90104969	A	19900316		199320
DE 3909153	C2	19930603	DE 3909153	A	19890321	G06F-015/18	199322

Priority Applications (No Type Date): DE 3909153 A 19890321
Cited Patents: NoSR.Pub; 3.Jnl.Ref; EP 377221
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
EP 388806	A					
Designated States (Regional): BE DE FR GB NL						
DE 3909153	C2		11			

Abstract (Basic): EP 388806 A
     A simultaneous computer structure for modelling and training
   artificial neuronal networks is linked to a host and formed from
   simple, identical processor elements as a two-dimensional **matrix** .
   These elements are supplied with a stream of commands from a sequencer
   according to the SIMD Principle. The elements set on the **matrix**
   diagonal are assigned to the neuronal network **nodes** and set apart for
   performing neurone functions. The non-diagonal processor elements take
   charge of the linking between the **nodes** and are set up for the
   function of the adjustable synaptic weightings.
     The **matrix** has a local adjacent network linked with the four
   immediately adjacent processors. Lines (38) lead separately from the
   neurone processors (28) in an x and y route destination. These select
   the non-diagonal synapse **processors** (30) **simultaneously** . In one
   destination these lines serve the accelerated distribution of
   computation results from the neurone processors to the synapse
   processors. In the other they serve the accelerated distribution of
   correction data during training.
     ADVANTAGE - Provides a simultaneous computer structure very well
   suited for installation, trials, testing and optimising free
   parameters. (11pp Dwg.No.4/6
Title Terms: PARALLEL; STRUCTURE; MODEL; TRAINING; NEUTRAL; NETWORK;
  SIGNIFICANT; EFFECT; **PERFORMANCE** ; LEARNING; ENVIRONMENT
Derwent Class: T01; T02
International Patent Class (Main): G06F-015/18
International Patent Class (Additional): G06F-015/80
File Segment: EPI

 14/5/45   (Item 45 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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008359632   **Image available**

WPI Acc No: 90-246633/199032
XRAM Acc No: C90-106548
XRPX Acc No: N90-191486
 **Triode array for superconducting neural network - comprises network array
 of opto-electric current-carrying filaments and controlled light source**
Patent Assignee: US SEC OF NAVY (USNA)
Inventor: SZU H H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week	
US 4943556	A	19900724	US 88252486	A	19880930		199032	B

Priority Applications (No Type Date): US 88252486 A 19880930

Abstract (Basic): US 4943556 A
        Parallel processing computer formed of an array of triodes
    comprises: 1-10000 parallel opto-electric current-carrying filaments
    and 1-10000 orthogonal similar filaments in physical but not electrical
    contact forming a triode array at the crossing **nodes** ; a controlled
    light supply to points of the first set of filaments just beyond the
    crossing **nodes** ; and means for receiving output signals from one set
    of filaments and supplying them to the light control to adjust the
    light pattern and provide iterative convergence towards a solution
  matrix based on the initialisation and the input. Pref. the filaments
    are made of superconducting material esp. YBa2Cu307.
        USE/ADVANTAGE - As a neural network for superconductive computers
    operating at cryogenic temps. in e.g. space, etc., which eliminates the
    'N-squared **bottleneck** ' of conventional technology. (9pp Dwg.No.3/5)
Title Terms: TRIODE; ARRAY; SUPERCONDUCTING; NEURAL; NETWORK; COMPRISE;
  NETWORK; ARRAY; OPTO; ELECTRIC; CURRENT; CARRY; FILAMENT; CONTROL; LIGHT;
  SOURCE
Derwent Class: L03; T01; U11; U14; U21; V07
International Patent Class (Additional): G06C-007/00
File Segment: CPI; EPI

 14/5/46   (Item 46 from file: 351)
DIALOG(R)File 351:DERWENT WPI
(c) 2000 Derwent Info Ltd. All rts. reserv.

008190026   **Image available**
WPI Acc No: 90-077027/199011
XRPX Acc No: N90-059176
 **Operating system down loading method for computer - using minimum boot
 control program which provides virtual disk connection to host**
Patent Assignee: NIPPON DIGITAL EQUIP KK (DIGI); DIGITAL EQUIP CORP (DIGI
)
Inventor: FLAHERTY J E; ABRAHAMS A
Number of Countries: 007 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week	
EP 358292	A	19900314	EP 89302132	A	19890303		199011	B
AU 8930887	A	19900315					199019	
US 5146568	A	19920908	US 88240955	A	19880906	G06F-013/14	199239	
CA 1321654	C	19930824	CA 592437	A	19890301	G06F-009/445	199340	
US 5280627	A	19940118	US 88240955	A	19880906	G06F-009/445	199404	
			US 92884078	A	19920515			
EP 358292	B1	19970910	EP 89302132	A	19890303	G06F-009/445	199741	
DE 68928311	E	19971016	DE 628311	A	19890303	G06F-009/445	199747	
			EP 89302132	A	19890303			

Priority Applications (No Type Date): US 88240955 A 19880906; US 92884078 A
  19920515

Cited Patents: 4.Jnl.Ref; A3...9035; No-SR.Pub
Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
EP 358292 A   E 14
   Designated States (Regional): DE FR GB NL
US 5146568 A   11
US 5280627 A   12 Div ex   US 88240955
                    Div ex   US 5146568
EP 358292 B1 E 19
   Designated States (Regional): DE FR GB NL
DE 68928311 E   Based on   EP 358292

Abstract (Basic): EP 358292 A
     In order to initialise a computer (10) which does not include a
local boot device, a minimum boot program is loaded from a host
computer (14) connected to the first computer by a communications
system (12).
     The mode being booted firstly broadcasts a boot request message
over the communications system. A host computer determines that it is
responsible for this function and down-loads a minimum boot control
program.
     the network device of the slave **node** loads the minimum control
program into the memory of the slave and activates the program. This
control program can move itself to the high end of the memory and link
itself into the start-up sequence.
     The normal self-test and boot system then continues but the boot
control program intercepts accesses to disc and provides disc access
from the host computer.
     ADVANTAGE - Allows booting with minimal knowledge of slave
Title Terms: OPERATE; SYSTEM; DOWN; **LOAD** ; METHOD; COMPUTER; MINIMUM; BOOT
 ; CONTROL; PROGRAM; VIRTUAL; DISC; CONNECT; HOST
Derwent Class: T01
International Patent Class (Main): G06F-009/445; G06F-013/14
International Patent Class (Additional): G06F-009/44; G06F-013/10;
G06F-015/16
File Segment: EPI

 14/5/47   (Item 47 from file: 351)
DIALOG(R)File 351:DERWENT WPI
(c) 2000 Derwent Info Ltd. All rts. reserv.

007873846   **Image available**
WPI Acc No: 89-138958/198919
XRPX Acc No: N89-106139
 Single node **imaging appts. for multi-processor network** node **- has at
least one network access method for containing** resources **for directing
data transport functions in and out of** node
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: HALIM N; NIKOLAOU C N; PERSHING J A
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
EP 314909	A	19890510	EP 88115361	A	19880920		198919 B
CA 1310428	C	19921117	CA 580819	A	19881020	G06F-015/16	199252
US 5191651	A	19930302	US 87116424	A	19871103	G06F-013/00	199311
			US 91682889	A	19910408		
EP 314909	B1	19950308	EP 88115361	A	19880920	G06F-015/16	199514
DE 3853257	G	19950413	DE 3853257	A	19880920	G06F-015/16	199520
			EP 88115361	A	19880920		

Priority Applications (No Type Date): US 87116424 A 19871103; US 91682889 A

19910408
Cited Patents: 3.Jnl.Ref; A3...9144; EP 118037
Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
EP 314909   A   E 24
   Designated States (Regional): DE FR GB
US 5191651 A   Cont of   US 87116424
EP 314909   B1 E 23
   Designated States (Regional): DE FR GB
DE 3853257 G   Based on   EP 314909

Abstract (Basic): EP 314909 A
     An apparatus for coupling a computer complex having several coupled
   processors in a **node** , the **node** being coupled to a data
   communication network having several **nodes** and a group of
   communication lines linking the **nodes** . The communication lines are
   grouped into transmission groups, each of the transmission groups
   including at least one of said transmission lines, the computer complex
   appearing to the network as a single **node** .
     One of the processors is designated a control processor including
   resource managers for controlling functions within one of said **nodes**
   (PU) and the others of the other processors being designated
   non-control processors. The non-control processors including at least
   one network access method (NAM) containing **resources** for directing
   data transport functions in and out of the **node** .
     2/10
Title Terms: SINGLE; **NODE** ; **IMAGE** ; APPARATUS; MULTI; PROCESSOR; NETWORK;
   NODE ; ONE; NETWORK; ACCESS; METHOD; CONTAIN; **RESOURCE** ; DIRECT; DATA;
   TRANSPORT; FUNCTION; **NODE**
Derwent Class: T01
International Patent Class (Main): G06F-013/00; **G06F-015/16**
File Segment: EPI

 14/5/48   (Item 48 from file: 351)
DIALOG(R)File 351:DERWENT WPI
(c) 2000 Derwent Info Ltd. All rts. reserv.

007866762
WPI Acc No: 89-131874/198918
XRPX Acc No: N89-100441
 Lighting model information processor for graphics **work station –**
 employs dynamic partitioning to balance computational workload **among**
 various parallel   processors **to avoid bottle-necks**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: GONZALEZ-LOPEZ J; HEMPEL B C; LIANG B C C; LIANG B C; LOPEZ J
Number of Countries: 006 Number of Patents: 005
Patent Family:
Patent No Kind Date   Applicat No Kind Date   Main IPC   Week
EP 314341   A   19890503 EP 88309573 A   19881013   198918 B
US 4866637 A   19890912   198946
CA 1304824 C   19920707 CA 581529   A   19881027 G06F-015/72   199233
EP 314341   B1 19950315 EP 88309573 A   19881013 G06T-011/00   199515
DE 3853336 G   19950420 DE 3853336   A   19881013 G06T-011/00   199521
                         EP 88309573 A   19881013

Priority Applications (No Type Date): US 87115467 A 19871030
Cited Patents: A3...9130; EP 193151; No.SR.Pub; US 4343037
Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
EP 314341   A   E 36
   Designated States (Regional): DE FR GB IT

EP 314341   B1 E 26
    Designated States (Regional): DE FR GB IT
DE 3853336 G   Based on   EP 314341

Abstract (Basic): EP 314341 A
        The system includes multiple floating point processing stages
    arranged and operated in pipeline. Each stage is constructed from one
    or more identical floating point processors. The system receives data
    representing coordinates in viewing space of **vertices** of a polygon
    and a normal at each of the **vertices** of the polygon. From that data
    coordinates of the **vertices** and screen colour intensity values
    associated with each **vertex** are calculated based upon a specified
    lighting model.
        Different processors may perform functions such as depth cueing,
    colour mapping and clipping from data representing ambient lighting and
    diffuse and specular reflection effects.
        USE/ADVANTAGE - Esp. in CAD/CAM High number of polygons processed
    per second means high **image** quality.
        5/5
Title Terms: LIGHT; MODEL; INFORMATION; PROCESSOR; **GRAPHIC** ; WORK; STATION
  ; EMPLOY; DYNAMIC; PARTITION; BALANCE; COMPUTATION; VARIOUS; PARALLEL;
  PROCESSOR; AVOID; BOTTLE; NECK
Index Terms/Additional Words: CAD; CAM
Derwent Class: T01
International Patent Class (Main): G06F-015/72; G06T-011/00
File Segment: EPI

 14/5/49   (Item 49 from file: 351)
DIALOG(R)File 351:DERWENT WPI
(c) 2000 Derwent Info Ltd. All rts. reserv.

007866283
WPI Acc No: 89-131395/198918
XRPX Acc No: N89-100105
 Aperiodic mapping method for interleaved devices - using bit matrix
 multiplication of logical address with predetermined matrix **to produce**
 physical address
Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: MCAULIFFE K P; MELTON E A; NORTON V A; PFISTER G F; WAKEFIELD S P
Number of Countries: 004 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week	
EP 313788	A	19890503	EP 88115088	A	19880915		198918	B
US 5111389	A	19920505	US 87114909	A	19871029		199221	
EP 313788	B1	19950621	EP 88115088	A	19880915	G06F-012/02	199529	
DE 3854035	G	19950727	DE 3854035	A	19880915	G06F-012/02	199535	
			EP 88115088	A	19880915			

Priority Applications (No Type Date): US 87114909 A 19871029
Cited Patents: 3.Jnl.Ref; A3...9031; EP 179401; No-SR.Pub; US 4400768
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
EP 313788	A	E	29			

    Designated States (Regional): DE FR GB
US 5111389 A   19
EP 313788   B1 E   23
    Designated States (Regional): DE FR GB
DE 3854035 G   Based on   EP 313788

Abstract (Basic): EP 313788 A
        The aperiodic mapping procedure for the mapping of logical to

physical addresses is defined as a permutation function for generating optimised stride accesses in an interleaved multiple device system such as a large, **parallel processing** shared memory system where the function comprises a bit-**matrix** multiplication of a presented first (logical) address with a predetermined **matrix** to produce a second (physical) address. The permutation function maps the address from a first to a second address space for improved memory **performance** . The memory has n logical address bits and 2 to the power d separately accessible memory devices and a second address that utilises n - d bits of the first address as the offset within the referenced device **node** .

A bit **matrix** multiplication is performed between successive rows of the **matrix** and bits of the first address to produce successive d bits of the second address.
USE/ADVANTAGE - Highly parallel systems. Enhances power of two stride access.
1/8
Title Terms: APERIODIC; MAP; METHOD; INTERLEAVED; DEVICE; BIT; **MATRIX** ; MULTIPLICATION; LOGIC; ADDRESS; PREDETERMINED; **MATRIX** ; PRODUCE; PHYSICAL; ADDRESS
Derwent Class: T01
International Patent Class (Additional): G06F-012/02; G06F-012/10
File Segment: EPI

 14/5/50   (Item 50 from file: 351)
DIALOG(R)File 351:DERWENT WPI
(c) 2000 Derwent Info Ltd. All rts. reserv.

007803882   **Image available**
WPI Acc No: 89-068994/198909
 CPU operating method for graphics **work-station - coupling CPU to**
  graphics **subsystem and controlling flow of** graphics **data and commands**
  to graphics pipeline **for** processing **and display**
Patent Assignee: DIGITAL EQUIP CORP (DIGI)
Inventor: ARMSTRONG W P; CARVER D C; DIPIRRO S D; DOYLE P L; ELLENBERGER J
  P; GEROVAC B J; GIBSON E S; JONES E O; ROACH W C; RUSHFORTH K C; SHAPIRO
  R E; RUTHERFORD K C; ELLENBERGE J P
Number of Countries: 012   Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
WO 8901664	A	19890223	WO 88US2727	A	19880812		198909 B
EP 329771	A	19890830	EP 88908489	A	19880812		198935
US 4928247	A	19900522	US 88184108	A	19880420		199024
JP 3501176	W	19910314	JP 88507486	A	19880512		199117
US 5097411	A	19920317	US 88258398	A	19881017		199214
US 5155822	A	19921013	US 8785081	A	19870813	G06F-012/00	199244
US 5251322	A	19931005	US 8785081	A	19870813	G06F-003/14	199341
			US 88184406	A	19880420		
			US 90477151	A	19900208		
EP 329771	B1	19960424	EP 88908489	A	19880812	G06T-017/00	199621
			WO 88US2727	A	19880812		
DE 3855234	G	19960530	DE 3855234	A	19880812	G06T-017/00	199627
			EP 88908489	A	19880812		
			WO 88US2727	A	19880812		

Priority Applications (No Type Date): US 8785081 A 19870813; US 88184108 A
  19880420; US 88184406 A 19880420; US 88258398 A 19881017; US 90477151 A
  19900208
Cited Patents: US 4315310; US 4509115; 1.Jnl.Ref
Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent

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WO 8901664  A  E 151
    Designated States (National): JP
    Designated States (Regional): AT BE CH DE FR GB IT LU NL SE
EP 329771   A  E
    Designated States (Regional): DE FR GB IT NL
US 5097411  A      45
US 5155822  A      34
US 5251322  A      46 Cont of         US 8785081
                      Cont of         US 88184406
                      Cont of                      US 5155822
EP 329771   B1 E   89 Based on                     WO 8901664
    Designated States (Regional): DE FR GB IT NL
DE 3855234  G         Based on                     EP 329771
                      Based on                     WO 8901664
```

Abstract (Basic): WO 8901664 A

    A central processing unit having associated system virtual memory is operated in connection with at least one operating device by providing a bus which couples the first central processing unit to at least one operating device. A reserved I/O space having starting and ending addresses on the bus is provided, as is a system virtual address space for at least one operating device within the system virtual memory. Mapping registers are provided in the operating device. The first central processing unit is operated to transfer the starting and ending addresses of the reserved I/O space on the bus to the mapping registers in the operating device.

    The CPU is operated to map the address space of the operating device into the system virtual address space. The CPU is operated to unprotect the system virtual address space where the address space of at least one operating device is mapped. The CPU can directly access the operating device without the need for direct memory access hardware, operating system calls, and device drivers.

    ADVANTAGE - High **performance** , multi-user capability.

    Dwg..1/14

Title Terms: CPU; OPERATE; METHOD; **GRAPHIC** ; WORK; STATION; COUPLE; CPU; **GRAPHIC** ; SUBSYSTEM; CONTROL; FLOW; **GRAPHIC** ; DATA; COMMAND; **GRAPHIC** ; PIPE; PROCESS; DISPLAY

Derwent Class: T01

International Patent Class (Main): G06F-003/14; G06F-012/00; G06T-017/00

International Patent Class (Additional): G06F-003/15; G06F-012/02; G06F-015/62; G06F-015/72

File Segment: EPI

 14/5/51   (Item 51 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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007748960
WPI Acc No: 89-014072/198902
XRPX Acc No: N89-010609
 Computer engineering graphs **modelling appts. - has outputs from code converters to count number of free** processors **in simulating** parallel **algorithms**
Patent Assignee: AS UKR PROB POWER M (AUPR-R)
Inventor: KUZMUK V V; LISITSYN E B; VASILEV V V
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
SU 1405070	A	19880623	SU 4150088	A	19861121		198902 B

Priority Applications (No Type Date): SU 4150088 A 19861121

45 May 10, 2000 10:16

Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
SU 1405070 A   10

Abstract (Basic): SU 1405070 A
        The circuitry contg. an input vectors comparator, an output vectors
    comparator, a modulo-2 adder, a logical adder, a multiplexer, memory, a
    set of models and two clock inputs, has each clock input connected to a
    corresp. code converter (9) and (10) with outputs to a reverse counter.

        USE/ADVANTAGE - In computer engineering for solving problems on
    Petry **graphs** and enabling algorithms for modelling of parallel
    processes to be debugged, **performance** is improved by provision to
    change the number of **vertices** of transitions which can be made in
    parallel. The new parts enable the number of triggered **vertex**
    -transition models to be limited independently of the number of
    inquiries for modelling. Implementation of parallel algorithms on
    different computing appts. can be simulated. Bul.23/23.6.88.
        1/6
Title Terms: COMPUTER; ENGINEERING; **GRAPH** ; MODEL; APPARATUS; OUTPUT; CODE
    ; CONVERTER; COUNT; NUMBER; FREE; PROCESSOR; SIMULATE; PARALLEL;
    ALGORITHM
Derwent Class: T01
International Patent Class (Additional): G06F-015/20
File Segment: EPI

 14/5/52   (Item 52 from file: 351)
DIALOG(R)File 351:DERWENT WPI
(c) 2000 Derwent Info Ltd. All rts. reserv.

007665368   **Image available**
WPI Acc No: 88-299300/198842
XRPX Acc No: N88-227021
 **Data-exchange system interface - has initial setting and adjusting inputs
 to logic switching units in two** triangular   matrices
Patent Assignee: KIEV ENG-CONS INST (KIEN-R); KIEV POLY (KIPO)
Inventor: KORNEICHUK V I; NAKALYUZHN A G; TARASENKO V P
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date   Applicat No Kind Date   Main IPC   Week
SU 1388882 A   19880415 SU 4122040   A   19860703   198842 B

Priority Applications (No Type Date): SU 4122040 A 19860703
Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
SU 1388882 A   4

Abstract (Basic): SU 1388882 A
        The circuit contg. groups (1,2) of interfacing units, a **matrix**
    (3) of switching units (4) and the groups of data inputs (7-10), has
    the **triangular   matrices** (5,6) of switching units (4) and the
    adjusting (15), initial setting (16) and sync. (17) inputs.
        In data-exchange between peripherals in a computing package, any
    pair of peripherals can be connected. Any two peripherals connected to
    the groups of interfacing units form an information communication
    channel by issuing the same codings. When the codings agree to a
    switching unit, switching of the channel takes place. The necessary
    channels between peripherals can be formed by adjustment when prepd. by
    a 1-level at the initial setting input.
        USE/ADVANTAGE - In computer engineering as an interface for
    data-exchange between peripherals. **Performance** is improved by any

pair of peripherals being connectible. Bul.14/15.4.88.
     1/2
Title Terms: DATA; EXCHANGE; SYSTEM; INTERFACE; INITIAL; SET; ADJUST; INPUT
  ; LOGIC; SWITCH; UNIT; TWO; **TRIANGLE** ; **MATRIX**
Derwent Class: T01
International Patent Class (Additional): **G06F-015/16**
File Segment: EPI

 14/5/53   (Item 53 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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007602591   **Image available**
WPI Acc No: 88-236523/198834
XRPX Acc No: N88-179730
 Raster display vector generator - uses triangular **logic** matrix **with
 line drawing unit to generate vector bits for direct masking of monitor
 screen**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: LUMELSKY L
Number of Countries: 005 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
EP 279227	A	19880824	EP 88101080	A	19880126		198834 B
US 4816814	A	19890328	US 8713848	A	19870212		198915
EP 279227	B1	19940518	EP 88101080	A	19880126	G09G-001/16	199420
DE 3889557	G	19940623	DE 3889557	A	19880126	G09G-001/16	199426
			EP 88101080	A	19880126		

Priority Applications (No Type Date): US 8713848 A 19870212
Cited Patents: A3...9116; EP 164880; No-SR.Pub; US 3906480; US 4580236; US
  4642625; WO 8500679
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
EP 279227	A	E	24			
Designated States (Regional): DE FR GB IT						
US 4816814	A		23			
EP 279227	B1	E	26			
Designated States (Regional): DE FR GB IT						
DE 3889557	G			Based on		EP 279227

Abstract (Basic): EP 279227 A
       The adaptor has a digital signal processor (10) utilised to manage
    the overall adapter's **resources** . The instruction and data store (12)
    is an instruction RAM which can be loaded with additional micro code
    for the signal processor, and also acts as a data RAM and provides the
    primary interface between signal processor (10) and the system
    processor. The data store (12) also performs the function of being a
    main store for the signal processor (10).
       A command F1FO register (14) serves as an input buffer for passing
    sequential commands to the digital signal processor (10) via an I/O bus
    (16) and, connects the video display adapter to the system or host
    processor. The pixel processor (18) contains logic that performs a
    number of display supporting functions such as line drawing
    manipulation which permits finite areas of the display screen to be
    manipulated.
       ADVANTAGE - Provides fast vector drawing independently of vector
    slope and position within screen area
Title Terms: RASTER; DISPLAY; VECTOR; GENERATOR; **TRIANGLE** ; LOGIC; **MATRIX**
  ; LINE; DRAW; UNIT; GENERATE; VECTOR; BIT; DIRECT; MASK; MONITOR; SCREEN
Derwent Class: P85; T04

International Patent Class (Main): G09G-001/16
International Patent Class (Additional): G09G-005/36
File Segment: EPI; EngPI

 14/5/54   (Item 54 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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007402593   **Image available**
WPI Acc No: 88-036528/198805
XRPX Acc No: N88-027595
 Data flow processing **elements in** parallel **computer architecture - has
 data flow elements interconnected by network which allows any processing
 element to send packets of information to any other element**
Patent Assignee: DATAFLOW COMPUTER CORP (DATA-N); DENNIS J B (DENN-I)
Inventor: DENNIS J
Number of Countries: 012   Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week	
WO 8800732	A	19880128	WO 87US1668	A	19870713		198805	B
AU 8779120	A	19880210					198819	
US 4814978	A	19890321	US 86885836	A	19860715		198914	
EP 315647	A	19890517	EP 87905809	A	19870713		198920	
JP 2500393	W	19900208	JP 87505215	A	19870713		199012	
EP 315647	A4	19910131	EP 87905809	A	19870000		199515	

Priority Applications (No Type Date): US 86885836 A 19860715
Cited Patents: 3.Jnl.Ref; US 4153932; US 4197589; US 4413318; US 4591979;
  US 4644461
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
WO 8800732	A	E	85			

    Designated States (National): AU JP
    Designated States (Regional): BE CH DE FR GB IT NL SE

Patent	Kind	Lan	Pg			
US 4814978	A		36			
EP 315647	A	E				

    Designated States (Regional): BE CH DE FR GB IT LI NL SE

Abstract (Basic): WO 8800732 A
      A static dataflow architecture uses many dataflow processing
   elements (110) to communicate by packets sent through a routing network
   (124) via paths (122). The routing instructions correspond to the modes
   of a directed **graph** in which any pair of **nodes** connected by an arc
   corresponds to a predecessor successor pair of instructions.
      Each predecessor instruction has one or more successor
   instructions, and each successor instruction has one or more
   predecessor instructions. The instructions include associations of
   execution components and enable components identified by instruction
   indices.
      ADVANTAGE - Uses VLSI chips to provide efficient high **performance**
   parallel computation.
Title Terms: DATA; FLOW; PROCESS; ELEMENT; PARALLEL; COMPUTER; ARCHITECTURE
 ; DATA; FLOW; ELEMENT; INTERCONNECT; NETWORK; ALLOW; PROCESS; ELEMENT;
 SEND; PACKET; INFORMATION; ELEMENT
Derwent Class: T01
International Patent Class (Additional): G06F-003/00; G06F-009/30;
 G06F-013/00; G06F-015/00
File Segment: EPI

 14/5/55   (Item 55 from file: 351)

DIALOG(R)File 351:DERWENT WPI
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007396212   **Image available**
WPI Acc No: 88-030147/198805
XRPX Acc No: N88-022567
 **Multiple CPU program management method for networking - comparing remote
 computer request with program** matrix **and list of currently running
 programs and accessed data files to grant access**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: CROSSLEY J F
Number of Countries: 006 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week	
EP 254854	A	19880203	EP 87108645	A	19870616		198805	B
BR 8703308	A	19880315					198816	
US 4780821	A	19881025	US 86890389	A	19860729		198845	
EP 254854	B1	19940302	EP 87108645	A	19870616	G06F-009/46	199409	
DE 3789175	G	19940407	DE 3789175	A	19870616	G06F-009/46	199415	
			EP 87108645	A	19870616			

Priority Applications (No Type Date): US 86890389 A 19860729
Cited Patents: 2.Jnl.Ref; A3...9019; EP 136666; GB 2062914; No-SR.Pub
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
EP 254854	A	E	20			
Designated States (Regional): DE FR GB IT						
US 4780821	A		18			
EP 254854	B1	E	20			
Designated States (Regional): DE FR GB IT						
DE 3789175	G			Based on		EP 254854

Abstract (Basic): EP 254854 A
     The multi-program management method comprises the steps of
converting a data management request originating at the server computer
or one of the remote computers into a file shaving and record locking
protocol request message. This message is then transmitted to the
server computer which determines whether the request message is to be
granted. A program **matrix** is established with entries indicating
whether a program can be run while another program or group of programs
are being run on the network.
     A list of programs is maintained which are currently being run on
the network and data files currently being accessed or otherwise not
available for access. The program **matrix** and list are then checked to
see if the request message poses a conflict with a currently running
program.
     ADVANTAGE - Allows program transfer without re-writing source code
Title Terms: MULTIPLE; CPU; PROGRAM; MANAGEMENT; METHOD; COMPARE; REMOTE;
 COMPUTER; REQUEST; PROGRAM; **MATRIX** ; LIST; CURRENT; RUN; PROGRAM; ACCESS
 ; DATA; FILE; ACCESS
Derwent Class: T01
International Patent Class (Main): G06F-009/46
International Patent Class (Additional): G06F-009/44; G06F-013/42;
 G06F-015/16
File Segment: EPI

 14/5/56   (Item 56 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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007254334

WPI Acc No: 87-251341/198736
XRPX Acc No: N87-188098
 Computer system esp. for simulation of biological processes - has matrix
 of node **processors interconnected via information and negator lines**
Patent Assignee: THOMAS G G (THOM-I)
Inventor: MITTERAUER B
Number of Countries: 008   Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
EP 235764	A	19870909	EP 87102829	A	19870227		198736 B
DE 3607241	A	19870910	DE 3607241	A	19860305		198737
US 4829451	A	19890509	US 8722256	A	19870305		198922
DE 3607241	C	19920416	DE 3607241	A	19860305		199216

Priority Applications (No Type Date): DE 3607241 A 19860305
Cited Patents: A3...8836; DE 3429078; EP 132926; No-SR.Pub; US 3473160; US
   4518866
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
EP 235764	A	G	33			

   Designated States (Regional): CH DE FR GB IT LI SE

US 4829451	A		15			
DE 3607241	C		16			

Abstract (Basic): EP 235764 A
       The main feature of the system is a central logic/processor unit
    (2) that is constructed as a **matrix** of **node** processors that are
    interconnected by information and rengator lines. Each mode processor
    has an input/processor control stage that is bus coupled to specific
    function processing units and a sub-**node** unit.
       Communication with the logic/processor unit is via an input module
    (1), peripherals (6) and a control unit (4). A bus (9,10) connects with
    an output module (3) with a coupled controller (5).
       ADVANTAGE - Provides greater memory and processing **capacity** .
    Accurate simulation of neuronal computation systems.
       3/7
Title Terms: COMPUTER; SYSTEM; SIMULATE; BIOLOGICAL; PROCESS; **MATRIX** ;
 NODE ; PROCESSOR; INTERCONNECT; INFORMATION; NEGATE; LINE
Derwent Class: T01
International Patent Class (Additional): **G06F-015/16** ; G06F-015/42
File Segment: EPI

 14/5/57   (Item 57 from file: 351)
DIALOG(R)File 351:DERWENT WPI
(c) 2000 Derwent Info Ltd. All rts. reserv.

004750210
WPI Acc No: 86-253551/198639
XRPX Acc No: N86-189615
 Data transmission switching system - has control establishing requested
 connection beginning at time based on prior established connections
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: FRANASZEK P A
Number of Countries: 007   Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
EP 195589	A	19860924	EP 86301778	A	19860312		198639 B
JP 61214694	A	19860924	JP 85283194	A	19851218		198645
US 4752777	A	19880621	US 8748982	A	19870512		198827
US 4814762	A	19890321	US 87125088	A	19871125		198914
CA 1263729	A	19891205					199002

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EP 195589   B1 19920610 EP 86301778  A  19860312 G06F-015/16   199224
DE 3685599  G  19920716 DE 3685599   A  19860312 G06F-015/16   199230
                        EP 86301778  A  19860312
US 34528    E  19940201 US 85713117  A  19850318 H04Q-001/00   199406
                        US 8748982   A  19870512
                        US 90541574  A  19900621
```

Priority Applications (No Type Date): US 85713117 A 19850318; US 8748982 A
    19870512; US 90541574 A 19900621
Cited Patents: 4.Jnl.Ref; A3...8929; No-SR.Pub
Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
EP 195589   A   E 22
    Designated States (Regional): DE FR GB IT
EP 195589   B1 E 28
    Designated States (Regional): DE FR GB IT
DE 3685599 G   Based on   EP 195589
US 34528   E   22 Cont of   US 85713117
                       Reissue of   US 4752777

Abstract (Basic): EP 195589 B
    The system includes a switching **matrix** (34) partitioned into
    selectable data transmission paths which provide connections between
    each of a no. of first parts of the **matrix** and selected ones of
    second ports of the **matrix** . First path controllers (30,40) control
    each data path for completing each selected connection. The system
    control (32,42) is responsive to a message requesting a connection
    between a first port and a selected second port to establish the
    requested connection.
    The system control establishes the requested connection·beginning
    at a determined time based on prior established connections to the
    selected second port. The path controllers establish the requested
    connection at the determined time.
    ADVANTAGE - High **throughput** control for wide band switching
    system. (22pp Dwg.No.3/19)
Title Terms: DATA; TRANSMISSION; SWITCH; SYSTEM; CONTROL; ESTABLISH;
  REQUEST; CONNECT; BEGIN; TIME; BASED; PRIOR; ESTABLISH; CONNECT
Derwent Class: T01; W01
International Patent Class (Main): **G06F-015/16** ; H04Q-001/00
International Patent Class (Additional): G06F-013/00; H04Q-003/68
File Segment: EPI

 14/5/58   (Item 58 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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004457649
WPI Acc No: 85-284527/198546
XRPX Acc No: N85-212096
 **Computer system for curve-solid classification and solid modelling -
 computes intersection of figures and solids represented as constructive
 solid geometry trees**
Patent Assignee: UNIV ROCHESTER (UYRP)
Inventor: ELLIS J L; KEDEM G
Number of Countries: 012 Number of Patents: 004
Patent Family:
Patent No Kind Date   Applicat No Kind Date   Main IPC   Week
EP 160848   A 19851113 EP 85104163 A 19850404   198546 B
US 4649498   A 19870310 US 84608295 A 19840508   198712
EP 160848   B1 19931201 EP 85104163 A 19850404 G06F-015/72 199348
DE 3587668   G 19940113 DE 3587668   A 19850404 G06F-015/72 199403

EP 85104163 A 19850404

Priority Applications (No Type Date): US 84608295 A 19840508
Cited Patents: 2.Jnl.Ref; A3...8840; No-SR.Pub
Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
EP 160848   A   E   99
    Designated States (Regional): AT BE CH DE FR GB IT LI LU NL SE
EP 160848   B1 E   67
    Designated States (Regional): AT BE CH DE FR GB IT LI LU NL SE
DE 3587668 G   Based on   EP 160848

Abstract (Basic): EP 160848 A
        A 1+log 2(N) by N grid or **array** (2) of **processors** is provided
    of which a bottom row is formed of N primitive classifiers (1). Each
    classifier is connected to a combine processor of the log 2(N) by N
    array . A combine **processor** at the top left **corner** is always a root
    processor and is connected to a direct memory access unit (4) which
    passes the output of the curve-solid classification system to a host
    main memory (6).
        An interface (3) allows the host computer (7) to read and write
    directly to the registers of the N primitive classifiers, to **load** the
    required recurrence coefficients into the registers. The functions
    computed by the primitive classifiers are: compute union; compute
    intersection; compute right input; compute bottom input; compute bottom
    input minus right input; pass information from the right; pass
    information from the bottom; and no-operation.
        USE - For **image** generation of solids on CRTs or hard copy
    printers. Used in computer-aided design and computer-assisted
    manufacturing applications, or for robot and machine tool simulation.
        6/29
Title Terms: COMPUTER; SYSTEM; CURVE; SOLID; CLASSIFY; SOLID; MODEL;
  COMPUTATION; INTERSECT; FIGURE; SOLID; REPRESENT; CONSTRUCTION; SOLID;
  GEOMETRY; TREE
Index Terms/Additional Words: ROBOT; TOOL; CAM; **IMAGE** ; CRT; PRINT
Derwent Class: P85; T01; T06; X25
International Patent Class (Main): G06F-015/72
International Patent Class (Additional): G09G-001/06
File Segment: EPI; EngPI

 14/5/59   (Item 59 from file: 351)
DIALOG(R)File 351:DERWENT WPI
(c) 2000 Derwent Info Ltd. All rts. reserv.

004327431
WPI Acc No: 85-154309/198526
XRPX Acc No: N85-116516
 **Data processing system for encoded control points - sends command to
   matrix maker card defining geometrical transformation to be performed on
   graphical   illustration**
Patent Assignee: BOSCH R CORP (BOSC)
Inventor: ANDREWS D H; LUCHT P H; PUTNAM L K
Number of Countries: 006 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
EP 146250	A	19850626	EP 84307611	A	19841105		198526 B
US 4646075	A	19870224	US 83548312	A	19831103		198710
CA 1238434	A	19880621					198832

Priority Applications (No Type Date): US 83548312 A 19831103
Cited Patents: 3.Jnl.Ref; A3...8746; No-SR.Pub; US 3763365; US 3816726; US

4208810
Patent Details:
Patent   Kind Lan Pg Filing Notes   Application Patent
EP 146250   A E 169
   Designated States (Regional): DE FR GB IT

Abstract (Basic): EP 146250 A
        A number of separate micro-programmed circuit cards is used, each
   of which is programmed to perform a specific processing operation. A
   command is first sent to a **matrix** maker card (201). This card,
   together with a **matrix** multiplier card (202), then calculates a
   transformation **matrix** representing the desired transformation.
        Electronic representations of control data points are then
   transmitted to the **pipeline** for **processing** and multipled by the
   transformation **matrix** , previously computed, in a vector multiplier
   circuit card (203). Next, the control points are clipped to the planes
   of a viewing frustum by a number of clipper cards (205-209).
        USE/ADVANTAGE - Reduces quantity of data needed to be stored to
   achieve real time animation. Increased processing speed. Does not need
   to convert curved portions into numerous line segments.
        2/9
Title Terms: DATA; PROCESS; SYSTEM; ENCODE; CONTROL; POINT; SEND; COMMAND;
 MATRIX ; MAKER; CARD; DEFINE; GEOMETRY; TRANSFORM; **PERFORMANCE** ;
 GRAPHICAL ; ILLUSTRATE
Derwent Class: P85; T01; W04
International Patent Class (Additional): G06F-009/28; G06F-015/34;
  G09G-001/16
File Segment: EPI; EngPI

 14/5/60   (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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05748515   **Image available**
DISTRIBUTED HYPER MEDIA SYSTEM

PUB. NO.:   10-031615 [JP 10031615 A]
PUBLISHED: February 03, 1998 (19980203)
INVENTOR(s): SHIMAMURA SAKAE
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP
              (Japan)
APPL. NO.:   08-205208 [JP 96205208]
FILED: July 16, 1996 (19960716)
INTL CLASS: [6] G06F-012/00; G06F-013/00; G06F-013/00; **G06F-015/16**
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 45.4
              (INFORMATION PROCESSING -- Computer Applications)

ABSTRACT
PROBLEM TO BE SOLVED: To suppress the **load** of directory server or network
in a distributed hyper media system formed for possessing **node** link
structure to be presented for supporting the navigation of user from the
directory server.

SOLUTION: A brousing device 40 is provided with a cache 18 for storing the
 node   link structure acquired from a directory server 20. When the
acquisition of contents of a certain **node** is requested from the user
through an input part 11, a contents possessing part 13 acquired the
contents of the relevant **node** from a distributed hyper media space 0 and
a contents output part 12 outputs these contents to the user. At the same
time, a communication part 15 for directory server first acquired only the
 node   link structure within the range linked from this acquired **node**

less than the prescribed number of link steps from the cache 18 but only when the **node** structure does not exist in the cache 18, it is possessed from the directory server 20 and a **node** link structure display part 14 makes this **node** structure into **graph** and presents it for the user.

14/5/61 **(Item 2 from file: 347)**
DIALOG(R)File 347:JAPIO
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05667490   **Image available**
METHOD AND DEVICE FOR LAYING OUT DATA IN DISTRIBUTED STORAGE TYPE PARALLEL
COMPUTERS

PUB. NO.:   09-282290 [JP 9282290 A]
PUBLISHED: October 31, 1997 (19971031)
INVENTOR(s):   SHINDO TATSUYA
               TAGUCHI KATSUHIKO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP
               (Japan)
APPL. NO.:   08-095749 [JP 9695749]
FILED: April 17, 1996 (19960417)
INTL CLASS: [6] **G06F-015/16** ; G06F-009/45
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 45.1
               (INFORMATION PROCESSING -- Arithmetic Sequence Units)

ABSTRACT

PROBLEM TO BE SOLVED: To reduce the burdens on programming and to improve the processing **performance** of distributed storage type parallel computers by automatically deciding the arrangement of parallelizable parts included in sequential programs at the time of parallellizing the sequential programs.

SOLUTION: A DBR **graph** for which DBRs (data layout basic areas) are made to **nodes** and the **nodes** are connected by directed branches in an execution order is generated (A1). The candidates of data layouts for plural PEs are listed for the respective DBRs in the DBR **graph** (A2) and a global alignment **graph** for which the respective candidates are the **nodes** and the **nodes** are connected by the directed branches by all combinations corresponding to the directed branches of the DBR **graph** is generated (A3). A shortest time route from a start point to an end point along the **nodes** and the directed branches in the global alignment **graph** is extracted (A4) and the data layout to the' plural PEs is performed corresponding to the candidates on the shortest time route (A5).

14/5/62 **(Item 3 from file: 347)**
DIALOG(R)File 347:JAPIO
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05630025   **Image available**
DECENTRALIZED PROCESSING SYSTEM

PUB. NO.:   09-244825 [JP 9244825 A]
PUBLISHED: September 19, 1997 (19970919)
INVENTOR(s):   HAMANO TAKAYOSHI
APPLICANT(s): FUJI XEROX CO LTD [359761] (A Japanese Company or
               Corporation), JP (Japan)
APPL. NO.:   08-049097 [JP 9649097]
FILED: March 06, 1996 (19960306)
INTL CLASS: [6] G06F-003/12; G06F-013/00; G06F-013/362; **G06F-015/16**
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 45.2

(INFORMATION PROCESSING -- Memory Units); 45.4 (INFORMATION PROCESSING -- Computer Applications)

ABSTRACT
PROBLEM TO BE SOLVED: To provide a decentralized processing system which eliminates a conflict of acquisition of a sequentially used common **resource** when plural processors which perform decentralized processes share the sequentially used common **resource** and allows the respective processors to use the sequentially used common **resource** in the order of the completion of the job processes.

SOLUTION: Respective S-FEP(slave Front End Processor) 15-17 before sending **image** data to a printer 18 send request-to-send messages to a scheduler 14, and send **image** data to the printer 18 after receiving OK-to-send messages from the scheduler 14. Here, the scheduler 14 manages the operation state and transmission state of the printer 18 by a printer state management part and sequentially processes job **nodes** that a transfer job management part manages according to the state of the printer 18.

14/5/63 **(Item 4 from file: 347)**
DIALOG(R)File 347:JAPIO
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05597539 **Image available**
SEMICONDUCTOR DEVICE AND ARITHMETIC OPERATION SYSTEM USING THE SAME, **IMAGE** PROCESSING SYSTEM, SOUND SIGNAL PROCESSING SYSTEM, PATTERN RECOGNITION SYSTEM, SIGNAL **PROCESSING** SYSTEM, **PARALLEL** DATA **PROCESSING** SYSTEM, AND VIDEO SIGNAL PROCESSING SYSTEM

PUB. NO.:   09-212339 [JP 9212339 A]
PUBLISHED: August 15, 1997 (19970815)
INVENTOR(s):   OMI TADAHIRO
                 OGAWA KATSUHISA
APPLICANT(s):   OMI TADAHIRO [000000] (An Individual), JP (Japan)
                 CANON INC [000100] (A Japanese Company or Corporation), JP
                 (Japan)
APPL. NO.:   08-013961 [JP 9613961]
FILED: January 30, 1996 (19960130)
INTL CLASS: [6] G06F-007/50; G06G-007/14; H03F-003/70; H03H-019/00
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units);
                 42.4 (ELECTRONICS -- Basic Circuits); 44.1 (COMMUNICATION --
                 Transmission Circuits & Antennae)
JAPIO KEYWORD:R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors,
                 MOS)

ABSTRACT
PROBLEM TO BE SOLVED: To constitute a large-scale highly parallel system, having operation elements coupled closely with one another, in one chip by using a device which has a floating **node** .

SOLUTION: **Capacity** means 8-13 are connected to input terminals 16-21 respectively. The common connection part between the uninverted input terminal 6 of a high-input-impedance operational amplifier 1 and **capacity** means 8-11, and the contact of the common connection part between the inverted input terminal 7 and **capacity** means 12-15 are floating **nodes** respectively. This arithmetic circuit comes into a signal operation mode wherein the signal from a precedent-stage operational amplifier 23 is received and processed when a reset signal 5 is negative. The gain setting of the operational amplifier 1 is determined by the **capacity** ratio of a **capacity** means 15 for negative feedback, and a grounded **capacity** means 14 and **capacity** means 8-13. By changing the **capacity** ratio, multi-valued linear operation is made possible.

 14/5/64   (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO
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05420050   **Image available**
METHOD FOR DISPLAYING **PERFORMANCE** DATA IN PARALLEL COMPUTER SYSTEM

PUB. NO.:   09-034850 [JP 9034850 A]
PUBLISHED: February 07, 1997 (19970207)
INVENTOR(s):   YAMAGA SUSUMU
                SAGAWA NOBUTOSHI
                OTA TADASHI
                TAKUBO SHUNJI
APPLICANT(s):   HITACHI LTD [000510] (A Japanese Company or Corporation), JP
                (Japan)
                HITACHI VLSI ENG CORP [489108] (A Japanese Company or
                Corporation), JP (Japan)
APPL. NO.:   07-185292 [JP 95185292]
FILED: July 21, 1995 (19950721)
INTL CLASS: [6] **G06F-015/16** ; G06F-003/153; G06T-011/20
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 45.3
                (INFORMATION PROCESSING -- Input Output Units); 45.9
                (INFORMATION PROCESSING -- Other)

ABSTRACT
PROBLEM TO BE SOLVED: To recognize distribution of accurate **performance**
 data intuitionally by plotting **performance**   data in the direction of
height of an axis orthogonal to a **picture** simulating each **node** of
parallel operation computers on a plane coordinate.

SOLUTION: A **picture** simulating computers on a plane coordinate is plotted
on a display screen 1 and **performance** data of collected parallel computer
system are converted and displayed in the direction of height of an axis.
orthogonal to the **picture** . In this case, a minimum unit of display is a
 node   and a network, and a **node** part is made up of, e.g. a frame 101, a
CPU 102, a memory 103, a reception amount 104 and a transmission amount
105, and the network is made up of a 1st communication channel 98, a 2nd
communication channel 99 and a router 100 and they are plotted. A thickness
in the direction of height of a displayed **image** in response to the
received **performance**   data is changed for each part except the frame 101
to represent the **performance**   data at that time. While expressing a
difference from each **node**   of the parallel computer system, a cross
reference with an actual indication is easily taken through the display
method as above.

 14/5/65   (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO
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05338373   **Image available**
VP **CAPACITY** CHANGING SYSTEM FOR ATM SWITCHING NETWORK

PUB. NO.:   08-293873 [JP 8293873 A]
PUBLISHED: November 05, 1996 (19961105)
INVENTOR(s):   NOZAKI MASANORI
                ISHIDA HIROSHI
                SUZUKI YUKIHIKO
                MATSUNAGA SATOHIKO
APPLICANT(s):   OKI ELECTRIC IND CO LTD [000029] (A Japanese Company or

Corporation), JP (Japan)
APPL. NO.: 07-117886 [JP 95117886]
FILED: April 19, 1995 (19950419)
INTL CLASS: [6] H04L-012/28; H04Q-003/00
JAPIO CLASS: 44.3 (COMMUNICATION -- Telegraphy); 44.4 (COMMUNICATION -- Telephone)

ABSTRACT

PURPOSE: To realize the quick reaction of VP **capacity** changing control.

CONSTITUTION: A repeating **node** 2 repeating plural VPs is provided with a connecting function part 30, an OAM cell copying part 41, the possibility of VP **capacity** change judging part 42 and a returning part 43. The connection function part 30 transfer-processes an OAM cell received from an upstream **node** to a down stream **node** . The OAM cell copying part 41 copies the OAM cell in **parallel** with the **processing** of the connecting function part 30. The possibility of VP **capacity** change judging part 42 extracts a control message from the OAM cell copied by the OAM cell copying part 41 to judge the possibility of changing the **capacity** . A returning part 43 transmits the juging result of the possibility of VP capacitor change judging part 42 to a transmission terminal **node** 1. A **capacity** change control part 11 in the transmission terminal **node** 1 judges the **capacity** change of VP from the transmission terminal **node** 1 to a terminating **node** 3 to be possible when the judging result from the repeating **node** 2 may **image** .

14/5/66 **(Item 7 from file: 347)**
DIALOG(R)File 347:JAPIO
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04961354 **Image available**
PARALLEL COMPUTER

PUB. NO.: 07-253954 [JP 7253954 A]
PUBLISHED: October 03, 1995 (19951003)
INVENTOR(s): OOTSUKA TATSUYUKI
YOSHIZAWA HIDEKI
FUJIMOTO KATSUTO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-042322 [JP 9442322]
FILED: March 14, 1994 (19940314)
INTL CLASS: [6] **G06F-015/16** ; **G06F-015/16**
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications)

ABSTRACT

PURPOSE: To perform processing at a high speed by eliminating the need for reallocating a processing program to a processor and rearrange data at the **time** of **execution** even when network constitution is altered.

CONSTITUTION: Respecitve **nodes** 1-(n) are each provided with >=2 processors PE1 and PE2. The processing program is allocated to the processors PE1 and PE2 in the order of the **nodes** 1-(n) without being made to correspond to the transfer direction of the data, which are arranged while made to correspond to the processors PE1 and PE2. When the data are transferred to the processors PE1 and PE2, the processors performs data arranged on the respective processors and the transferred data to perform processing for finding the product of a **matrix** , etc. The processors are allocated in the order of the **nodes** , so the network constitution can easily be altered. Even when the network constitution is altered, the need to rearrange the data at the **time** of the **execution** is eliminated and

the processing is performed at a high speed.

 14/5/67   (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO
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04518073   **Image available**
PROGRAM DEVELOPING SYSTEM FOR PARALLEL COMPUTERS

PUB. NO.:   06-161973 [JP 6161973 A]
PUBLISHED: June 10, 1994 (19940610)
INVENTOR(s):   OGAMI YASUHIRO
APPLICANT(s): SANYO ELECTRIC CO LTD [000188] (A Japanese Company or
               Corporation), JP (Japan)
APPL. NO.:   04-311604 [JP 92311604]
FILED: November 20, 1992 (19921120)
INTL CLASS: [5] **G06F-015/16** ; G06F-009/06; G06F-009/45
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 45.1
               (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 1799, Vol. 18, No. 489, Pg. 67,
               September 12, 1994 (19940912)

ABSTRACT
PURPOSE: To attain the direct use of accumulated software **resources** by
converting each processing content to the processing code of machine
language level by a conversion means, and automatically generating the
execution codes of parallel computers by an execution code generating
means.

CONSTITUTION: A flow chart analysis part 12 identifies dependence for each
 node   and between the **nodes** and another information from a **graphic** , a
line, and a character described on an inputted flow .chart. Either of
conversion parts 16a-16e in accordance with the respective processing
content of the **node**   and another information identified by the flow
analysis part 12 is selected by a conversion decision part 14, then,
conversion is performed. One execution code can be generated from plural
conversion results obtained by the conversion parts 16a-16e which convert
the processing content of the **node** to the processing code of machine
language level corresponding to a decision result by an execution code
generating part 30.

 14/5/68   (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO
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04477453   **Image available**   -
MATRIX NETWORK CIRCUIT

PUB. NO.:   06-121353 [JP 6121353 A]
PUBLISHED: April 28, 1994 (19940428)
INVENTOR(s):   ENDO KANICHI
               YAMANAKA NAOAKI
               DOI YUKIHIRO
               GENDA KOICHI
APPLICANT(s): NIPPON TELEGR & TELEPH CORP <NTT> [000422] (A Japanese
               Company or Corporation), JP (Japan)
APPL. NO.:   04-265032 [JP 92265032]
FILED: October 02, 1992 (19921002)
INTL CLASS: [5] H04Q-003/52; H04Q-003/52; H04L-012/48
JAPIO CLASS: 44.4 (COMMUNICATION -- Telephone); 44.3 (COMMUNICATION --

ABSTRACT
PURPOSE: To reduce the entire contention arbitration time and a transfer
path for various data by forming a large scale **matrix** switch with sets of
lots of small scale **matrix** switches and processing contention arbitration
in **parallel** through divided **processing** .

CONSTITUTION: Groups of divided request generating sources R1-R8 and
resources S1-S8 are mutually connected by each of small scale **matrix**
switches G(1, 1)-G(4, 4) respectively. Through the constitution above,
access requests and/or data from the request generating sources R1-R8 are
directly transferred to the **matrix** switches G(1, 1)-G(4, 4)
interconnected by input side connection lines L1-L8, and the access
requests and/or data from the **matrix** switches G(1, 1)-G(4, 4) to the
resources S1-S8 are directly transferred to the **resources**   S1-S8
interconnected by output side connection lines LO1-LO8. Thus, number of
passing **cross**   **points**   is decreased and the contention arbitration is
implemented in parallel by using each small scale **matrix** switch, then the
entire processing speed is quickened.

 14/5/69   **(Item 10 from file: 347)**
DIALOG(R)File 347:JAPIO'
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ABSTRACT
PURPOSE: To efficiently process a finite element method in a parallel
computer.

CONSTITUTION: A region of analysis is divided into finite elements in a
procedure 1. Respective element matrixes corresponding to respective finite
elements are prepared in **parallel** by respective **processor** elements in a
state where the respective finite elements are allocated to the respective
processor elements in the parallel computer in a procedure 2. Respective
pieces of data in the respective element matrixes and the members of **nodes**
 generating the respective elements are transferred to the respective
processor elements taking charge of the **node** numbers and data on the
element matrixes are added in the processor element in charge of the
respective **nodes**   in parallel so as to efficiently generate a global
 matrix   at high speed in a state where the respective **nodes** are
allocated to the respective processor elements in a procedure 3. Wasteful
data transfer at the time of solving an equation expressed by the **matrix**
 is eliminated by using the number of the **node** making the element
transferred at the time of preparing the global **matrix** for data transfer

in a procedure 4.

 14/5/70   (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO
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03846758   **Image available**
DEVICE AND METHOD FOR DIVIDING DATA FLOW **GRAPH**

PUB. NO.:   04-211858 [JP 4211858 A]
PUBLISHED: August 03, 1992 (19920803)
INVENTOR(s): MUNAKATA KOICHI
              INAOKA MIE
              SHIMA KENJI
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or
              Corporation), JP (Japan)
APPL. NO.:   03-063752 [JP 9163752]
FILED: March 06, 1991 (19910306)
INTL CLASS: [5] **G06F-015/16**
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications)
JOURNAL: Section: P, Section No. 1454, Vol. 16, No. 555, Pg. 94,
              November 25, 1992 (19921125)

ABSTRACT
PURPOSE: To reduce influence upon processing **execution time** due to
communication between processors by allocating each **node** of a data flow
 graph so that the number of pockets to flow between the processors
becomes small.

CONSTITUTION: In respect of an objective **node** to be allocated selected by
a next allocated **node** selecting means 14, a preceding **node** to output an
arc to be inputted to the objective **node** to be allocated is searched by a
preceding **node** searching means 15. Next, the processor allocated to the
preceding **node** is searched by a searching means 16 for the processor
allocated to the preceding **node** . The processor is allocated to the
objective **node** to be allocated by an allocated processor determining
means 4 according to the allocating state of the processor so that the
number of the packets to flow between the processors becomes small. Then,
the data flow **graph** is divided.

 14/5/71   (Item 12 from file: 347)
DIALOG(R)File 347:JAPIO
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03748373   **Image available**
METHOD AND DEVICE FOR WIRING BETWEEN ELEMENTS

PUB. NO.:   04-113473 [JP 4113473 A]
PUBLISHED: April 14, 1992 (19920414)
INVENTOR(s): DATE HIROSHI
              HAYASHI TERUMINE
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
              (Japan)
APPL. NO.:   02-232325 [JP 90232325]
FILED: September 04, 1990 (19900904)
INTL CLASS: [5] G06F-015/60; H01L-021/82; H05K-003/00
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 42.1
              (ELECTRONICS -- Electronic Components); 42.2 (ELECTRONICS --
              Solid State Components)
JAPIO KEYWORD:R129 (ELECTRONIC MATERIALS -- Super High Density Integrated

JOURNAL:
Circuits, LSI & GS
Section: P, Section No. 1397, Vol. 16, No. 365, Pg. 151,
August 06, 1992 (19920806)

ABSTRACT
PURPOSE: To execute large scale wiring processing with memory small in
capac ity at high speed by executing route decision at every grating unit
in each small area of rough wiring route in each small area in parallel.

CONSTITUTION: A CPU21 generalizes the whole operation, and processors(PE)
22a-22d, 23a-23h perform **parallel processing** at each processing stage,
and they are connected in hierarchical fashion, and are connected to shared
memory 20, 24a-24d, and 25. In such a case, a division area in which a
wiring area is divided is divided into the small areas, hence, each of the
small areas is set as a **node** , and a **graph** provided with a branch
between points in accordance with the small area is generated when
neighboring relation exists between the small areas. The route between the
small areas is retrieved from the connection relation of the **graph** , and
it is set as the rough wiring route, and finally, detail wiring is
performed in parallel at every small unit on the rough wiring route.
Thereby, it is possible to execute retrieval between elements in a large
scale wiring area at high speed, and to reduce required memory **capacity** .

14/5/72   (Item 13 from file: 347)
DIALOG(R)File 347:JAPIO
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02896432   **Image available**
PARALLEL COMPILING METHOD

PUB. NO.:   01-194032 [JP 1194032 A]
PUBLISHED: August 04, 1989 (19890804)
INVENTOR(s):   TANAKA TERUO
                IHARA SHIGEO
                HAMANAKA NAOKI
                IWAZAWA KYOKO
APPLICANT(s):   HITACHI LTD [000510] (A Japanese Company or Corporation), JP
                (Japan)
APPL. NO.:   63-017072 [JP 8817072]
FILED: January 29, 1988 (19880129)
INTL CLASS: [4] G06F-009/44; **G06F-015/16**
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units);
                45.4 (INFORMATION PROCESSING -- Computer Applications)
JOURNAL: Section: P, Section No. 954, Vol. 13, No. 488, Pg. 75,
                November 07, 1989 (19891107)

ABSTRACT
PURPOSE: To guarantee the uniformity of data discriminators by checking the
flow of processing such as the loop structure of respective processors at
the **time** of compiling, **executing** SEND processing and RECEIVE processing
and developing the loop structure until the uniformity is held.

CONSTITUTION: Different data discriminators are assigned 2 to respective
combinations of all SEND and RECEIVE processing expressed on a program. An
S pole for executing the SEND processing, an R **node** for executing the
RECEIVE processing, a converging point **node** for expressing loop
structure, and a branch processing **node** are extracted to form a control
flow **graph** 6. The control flow **graph** 6 expresses the order relation of
program execution processing. All corresponding combinations of S and R
nodes included in the loop structure are reversely searched and whether
the execution of an R **node** corresponding to the i-th loop is ended or not

prior to the S **node** in the i-th loop can be executed. When said R **node** is not executed, the loop is developed twice. Consequently, uniformity of data discriminators indicating the correspondence between the SEND processing and RECEIVE processing can be guaranteed.

14/5/73   (Item 14 from file: 347)
DIALOG(R)File 347:JAPIO
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02778672   **Image available**
SIMULTANEOUS EQUATIONS CALCULATING METHOD BY VECTOR CALCULATOR

PUB. NO.:   01-076272 [JP 1076272 A]
PUBLISHED: March 22, 1989 (19890322)
INVENTOR(s):   ORII SHIGEO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP
               (Japan)
APPL. NO.:   62-234172 [JP 87234172]
FILED: September 18, 1987 (19870918)
INTL CLASS: [4] G06F-015/324; G06F-015/347
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications)
JOURNAL: Section: P, Section No. 895, Vol. 13, No. 297, Pg. 75, July
               10, 1989 (19890710)

ABSTRACT
PURPOSE: To shorten a **load** /storing time and to attain high speed calculation by processing with a long vector length consisting of a connecting register in the data processing of a column direction and processing with a length corresponding to a row consisting of a division register in the operation of the row and the row.

CONSTITUTION: In the **processing** P1, the **vector** registers are connected a coefficient **matrix** is loaded with the long vector length, namely, a(sub 11)-a(sub nn) are integrally loaded. Then, in the processing P2, the elements of the coefficients disposed at an equal interval on the coefficient **matrix** are collected to a series of registers by the use of the mask of the pattern of the equal interval. In a P3, the constitution of the register is changed to the data of one row match the data of one row to one vector register. Then, in a P4, a discharge calculation for bringing the element of a partial coefficient to '0' on the reconstituted register is executed. These processings P1-P4 are repeated on all the rows. According to the processings, the coefficient **matrix** goes to a **triangle matrix** as a discharge calculation result R. In such a way, data is stored in the register as much as possible to reduce the number of memory accesses and shorten the **load** / storing time.

14/5/74   (Item 15 from file: 347)
DIALOG(R)File 347:JAPIO
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02255561   **Image available**
EXCLUSIVELY USED PROCESSOR

PUB. NO.:   62-172461 [JP 62172461 A]
PUBLISHED: July 29, 1987 (19870729)
INVENTOR(s):   DOI TAKASHI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP
               (Japan)
APPL. NO.:   61-014126 [JP 8614126]
FILED: January 24, 1986 (19860124)

ABSTRACT

PURPOSE: To equalize a **load** of a processor by successively forward and
backward substituting an LU decomposed **matrix** of respective factor
matrices to vector data inputted from a repetition calculation circuit by
a forward and backward substitution circuit and performing a reverse
matrix operation of an approximate **matrix** .

CONSTITUTION: In an asymmetrical linear equation obtained by approximating
five point differences of a two-dimensional advection diffusion equation
applied on a rectangular area, the equation to be solved is represented by
an equation 1. When an integral vector is considered to be U and a
difference equation is represented as A.u=f, A has the structure as shown
in the figure, D corresponds to D of the equation 1, Ax to Axl, and Ay to
Ayl, Ayu, respectively. The **matrix** A is inputted by a signal line 11 and
the vector (f) is inputted and in a factor **matrix** decomposing circuit 1,
lower **triangle** **matrices** Lx, L, y and upper **triangle** **matrices** Ux, Uy
are calculated. Thereby, when a pipe line system is used in the processor,
it is not required to use a list vector system and when a **parallel**
 processor system is used, the number of the operations capable being
executed in parallel is made constant and the equality in the **load** of the
operation processor can be maintained.
?

```
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```

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Set     Items    Description
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                 SIMULTANEOUS?)(2N)(PROCESSOR? ? OR PROCESSING OR SERVER)
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S3    6046698    CAPACITY OR PERFORMANCE OR LOAD OR EXECUT?(2N)TIME? ? OR R-
                 ESOURCE? ? OR THROUGHPUT OR THROUGH()PUT OR TRAFFIC OR CONCUR-
                 RENCY OR BOTTLENECK? ? OR TRACE()TOOL? ? OR STATISTIC? ? OR W-
                 ORKLOAD OR CLUSTER(2N)MANAG? OR DATA()HANDLING
S4    4930014    GRAPH? OR VISUAL? OR PICTORIAL OR PICTURE OR 3()D OR THREE-
                 ()DIMENSIONAL OR 3D OR IMAGE OR IMAGES OR ILLUSTRATION OR X()Y
                 OR XY OR MATRIX OR MATRICES
S5     499733    NODE OR NODES OR VERTEX OR VERTICES OR CORNER OR TRIANGULAR
                 OR TRIANGLE? ? OR CROSS()POINT? ? OR CROSSPOINT? ? OR FORK? ?
S6       2514    (S1 OR S2) AND S3 AND S4 AND S5
S7        877    (S1 OR S2)(S)S3(S)S4(S)S5
S8     219967    S4(5N)(REPRESENTATION OR VISUALIZATION OR VISUALISATION)
S9        124    (S1 OR S2) AND S3 AND S5 AND S8
S10       106    S9 AND PY<1998
```

S11   69   RD (unique items)
?t11/7/all

11/7/1   (Item 1 from file: 108)
DIALOG(R)File 108:Aerospace Database
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02296574   N97-16993
   Visualization **of Unsteady Computational Fluid Dynamics**
   Final Report
   HAIMES, ROBERT; et al.
   Massachusetts Inst. of Tech., Cambridge, MA. Computational Aerospace
Sciences lab.
   CORPORATE CODE: MJ700802
   Mar. **1997**   41P.
   REPORT NO.: NASA-CR-203964; NAS 1.26:203964; NIPS-97-21356
   CONTRACT NO.: NAG2-884
   LANGUAGE: English
   COUNTRY OF ORIGIN: United States   COUNTRY OF PUBLICATION: United States
   DOCUMENT TYPE: REPORT
   DOCUMENTS AVAILABLE FROM AIAA Technical Library
   OTHER AVAILABILITY: CASI HC A03/MF A01
   JOURNAL ANNOUNCEMENT: STAR9701
   The current compute environment that most researchers are using for the
calculation of 3D unsteady Computational Fluid Dynamic (CFD) results is a
super-computer class machine. The Massively **Parallel   Processors (MPP**
's) such as the 160 **node** IBM SP2 at NAS and clusters of workstations
acting as a single **MPP** (like NAS's SGI Power-Challenge array and the J90
cluster) provide the required computation bandwidth for CFD calculations of
transient problems. If we follow the traditional computational analysis
steps for CFD (and we wish to construct an interactive visualizer) we need
to be aware of the following: (1) Disk space requirements. A single
snap-shot must contain at least the values (primitive variables) stored at
the appropriate locations within the mesh. For most simple 3D Euler solvers
that means 5 floating point words. Navier-Stokes solutions with turbulence
models may contain 7 state-variables. (2) Disk speed vs. Computational
speeds. The time required to read the complete solution of a saved time
frame from disk is now longer than the compute time for a set number of
iterations from an explicit solver. Depending, on the hardware and solver
an iteration of an implicit code may also take less time than reading the
solution from disk. If one examines the **performance** improvements in the
last decade or two, it is easy to see that depending on disk **performance**
 (vs. CPU improvement) may not be the best method for enhancing
interactivity. (3) Cluster and Parallel Machine I/O problems. Disk access
time is much worse within current parallel machines and cluster of
workstations that are acting in concert to solve a single problem. In this
case we are not trying to read the volume of data, but are running the
solver and the solver outputs the solution. These traditional network
interfaces must be used for the file system. (4) Numerics of particle
traces. Most **visualization** tools can work upon a single snap shot of the
data but some **visualization** tools for transient problems require dealing
with time. (Derived from text)
   SOURCE OF ABSTRACT/SUBFILE: NASA CASI

11/7/2   (Item 2 from file: 108)
DIALOG(R)File 108:Aerospace Database
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02295471   N97-15577
 Flexibility and Performance **of Parallel File Systems**
   KOTZ, DAVID; NIEUWEJAAR, NILS; et al.

                    2 May 10, 2000 10:56

Dartmouth Coll., Hanover, NH. Dept. of Computer Science
CORPORATE CODE: DB608495
PLACE OF PUBLICATION: Germany PUBLISHER: Springer-VerlagJan. **1996**
12P.
PRESENTATION NOTE: Presented at International Conference of the Austrian
Center for Parallel Computation (ACPC)
REPORT NO.: NASA-CR-203565; NAS 1.26:203565; NIPS-97-13269
CONTRACT NO.: NCC2-849; NAG2-936; NSF CCR-94-04919
LANGUAGE: English
COUNTRY OF ORIGIN: United States COUNTRY OF PUBLICATION: Germany
DOCUMENT TYPE: REPRINT
DOCUMENTS AVAILABLE FROM AIAA Technical Library
OTHER AVAILABILITY: CASI HC A03/MF A01
JOURNAL ANNOUNCEMENT: STAR9701

As we gain experience with parallel file systems, it becomes increasingly clear that a single solution does not suit all applications. For example, it appears to be impossible to find a single appropriate interface, caching policy, file structure, or disk-management strategy. Furthermore, the proliferation of file-system interfaces and abstractions make applications difficult to port. We propose that the traditional functionality of parallel file systems be separated into two components: a fixed core that is standard on all platforms, encapsulating only primitive abstractions and interfaces, and a set of high-level libraries to provide a variety of abstractions and application-programmer interfaces (API's). We present our current and next-generation file systems as examples of this structure. Their features, such as a three-dimensional file structure, strided read and write interfaces, and I/O-**node** programs, are specifically designed with the flexibility and **performance** necessary to support a wide range of applications. (Author)

11/7/3   (Item 3 from file: 108)
DIALOG(R)File 108:Aerospace Database
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02244300 N96-18401
 Runtime volume visualization **for parallel CFD**
  Final Report
  MA, KWAN-LIU
  Institute for Computer Applications in Science and Engineering, Hampton,
VA.
  CORPORATE CODE: IJ535353
  Oct. **1995**   14P.
  PUBLICATION NOTE: Submitted for publication in Proceedings of the
Parallel CFD 1995 Conference
  PRESENTATION NOTE: Presented at the Parallel CFD 1995 Conference, United
States
  REPORT NO.: NASA-CR-198232; NAS 1.26:198232; ICASE-95-74; NIPS-96-07901
  CONTRACT NO.: NAS1-19480; RTOP 505-90-52-01
  LANGUAGE: English
  COUNTRY OF ORIGIN: United States COUNTRY OF PUBLICATION: United States
  DOCUMENT TYPE: PREPRINT
  DOCUMENTS AVAILABLE FROM AIAA Technical Library
  OTHER AVAILABILITY: CASI HC A03/MF A01
  JOURNAL ANNOUNCEMENT: STAR9605
  This paper discusses some aspects of design of a data distributed, massively parallel volume rendering library for runtime **visualization** of parallel computational fluid dynamics simulations in a message-passing environment. Unlike the traditional scheme in which **visualization** is a postprocessing step, the rendering is done in place on each **node** processor. Computational scientists who run large-scale simulations on a massively parallel computer can thus perform interactive monitoring of

their simulations. The current library provides an interface to handle volume data on rectilinear grids. The same design principles can be generalized to handle other types of grids. For demonstration, we run a parallel Navier-Stokes solver making use of this rendering library on the Intel Paragon XP/S. The interactive visual response achieved is found to be very useful. **Performance** studies show that the parallel rendering process is scalable with the size of the simulation as well as with the parallel computer. (Author)

 11/7/4   (Item 4 from file: 108)
DIALOG(R)File 108:Aerospace Database
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02136013   N94-21622
 A data distributed, parallel algorithm for ray-traced volume rendering
  MA, KWAN-LIU; PAINTER, J. S.; HANSEN, C. D.; KROGH, M. F.
  Los Alamos National Lab., NM.
  CORPORATE CODE: L4405312
  Mar. **1993**   35P.
  PRESENTATION NOTE: Presented at the Parallel Rendering Symposium, San Jose, CA, 25 Oct. 1993
  REPORT NO.: DE93-040150; LA-UR-93-3138; CONF-9310153-1
  CONTRACT NO.: W-7405-ENG-36
  LANGUAGE: English
  COUNTRY OF ORIGIN: United States   COUNTRY OF PUBLICATION: United States
  DOCUMENT TYPE: CONFERENCE PAPER
  DOCUMENTS AVAILABLE FROM AIAA Technical Library
  OTHER AVAILABILITY: CASI HC A03/MF A01
  JOURNAL ANNOUNCEMENT: STAR9405
  This paper presents a divide-and-conquer ray-traced volume rendering algorithm and its implementation on networked workstations and a massively parallel computer, the Connection Machine CM-5. This algorithm distributes the data and the computational **load** to individual processing units to achieve fast, high-quality rendering of high-resolution data, even when only a modest amount of memory is available on each machine. The volume data, once distributed, is left intact. The processing **nodes** perform local ray-tracing of their sub-volume concurrently. No communication between processing units is needed during this locally ray-tracing process.
  A sub-image is generated by each processing unit and the final image is obtained by compositing sub-images in the proper order, which can be determined a priori. Implementations and tests on a group of networked workstations and on the Thinking Machines CM-5 demonstrate the practicality of our algorithm and expose different **performance** tuning issues for each platform. We use data sets from medical imaging and computational fluid dynamics simulations in the study of this algorithm (DOE)
  SOURCE OF ABSTRACT/SUBFILE: DOE

 11/7/5   (Item 5 from file: 108)
DIALOG(R)File 108:Aerospace Database
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02043413   N92-27677
 Aspects of unstructured grids and finite-volume solvers for the Euler and Navier-Stokes equations
  BARTH, TIMOTHY J.
  National Aeronautics and Space Administration. Ames Research Center, Moffett Field, CA.
  CORPORATE CODE: NC473657
  In AGARD, Special Course on Unstructured Grid Methods for Advection Dominated Flows 61 p (SEE N92-27671 18-34)

May **1992**
LANGUAGE: English
COUNTRY OF ORIGIN: United States   COUNTRY OF PUBLICATION: United States
DOCUMENT TYPE: CONFERENCE PAPER
DOCUMENTS AVAILABLE FROM AIAA Technical Library
OTHER AVAILABILITY: CASI HC A04/MF A03
JOURNAL ANNOUNCEMENT: STAR9218
    One of the major achievements in engineering science has been the development of computer algorithms for solving nonlinear differential equations such as the Navier-Stokes equations. In the past, limited computer **resources** have motivated the development of efficient numerical schemes in computational fluid dynamics (CFD) utilizing structured meshes. The use of structured meshes greatly simplifies the implementation of CFD algorithms on conventional computers. Unstructured grids on the other hand offer an alternative to modeling complex geometries. Unstructured meshes have irregular connectivity and usually contain combinations of **triangles** , quadrilaterals, tetrahedra, and hexahedra. The generation and use of unstructured grids poses new challenges in CFD. The purpose of this note is to present recent developments in the unstructured grid generation and flow solution technology (H.A.)
    SOURCE OF ABSTRACT/SUBFILE: NASA CASI

11/7/6   (Item 6 from file: 108)
DIALOG(R)File 108:Aerospace Database
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01967133   N91-21757
 Computer aided design tools and algorithms for submicron technologies
  Final Report, 1 Jul. 1987 - 30 Jun. 1990
  DUTTON, ROBERT W.
  Stanford Univ., CA.
  CORPORATE CODE: S0380476
  Oct. **1990**   13P.
  REPORT NO.: AD-A231171; ARO-24863.13-EL
  CONTRACT NO.: DAAL03-87-K-0077
  LANGUAGE: English
  COUNTRY OF ORIGIN: United States   COUNTRY OF PUBLICATION: United States
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  OTHER AVAILABILITY: CASI HC A03/MF A01
  JOURNAL ANNOUNCEMENT: STAR9113
    Advanced algorithms for two and three dimensional modeling of semiconductor devices have been developed, implemented on parallel computers and tested using several high **performance** technologies. Computational limitations for semiconductor device analysis have been extended to greater than 100000 **nodes** and speedup factors greater than 10-fold have been realized using distributed memory (MIMD) architectures. Two classes of algorithms have been explored using **parallel processing** -distributed multifrontal (DMF) and Monte Carlo (MC). The DMF algorithm has been implemented and tested for 3D device analysis of MOS, bipolar and latchup examples using iterative methods for single- and two-carrier transport. A windowed MC analysis of 2D hot carrier effects in Si MOS and GaAs MESFET devices has been achieved on several parallel architectures with near ideal speedup factors up to 20 processors. Useability of device simulation has been enhanced and demonstrated through applications. The range of technologies that can be modeled with the 2D PISCES program now includes: GaAs, GeSi heterojunctions and photo- and other carrier-generation process. Moreover, layout-driven input 2D/**3D** output **visualization** capabilities increase user efficiency. Device and technology scaling applications have been used to evaluate both 2D and 3D device capabilities. BiCMOS scaling issues and new structures have been

evaluated using PISCES and mixed-mode (device circuit) capabilities (DTIC)
    SOURCE OF ABSTRACT/SUBFILE: DTIC

 11/7/7   (Item 7 from file: 108)
DIALOG(R)File 108:Aerospace Database
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01925328   A91-26933
 Systolic array designs for Kalman filtering
  KUNG, SUN-YUAN (Princeton University, NJ); HWANG, JENQ-NENG (Washington,
University, Seattle)
  IEEE Transactions on Signal Processing (ISSN 1053-587X), vol. 39, Jan.
1991, p. 171-182. SDIO-supported research.
  Jan. **1991**   24 REFS.
  CONTRACT NO.: NSF MIP-87-14689; N00014-88-K-0515
  LANGUAGE: English
  COUNTRY OF ORIGIN: United States   COUNTRY OF PUBLICATION: United States
  DOCUMENT TYPE: JOURNAL ARTICLE
  DOCUMENTS AVAILABLE FROM AIAA Technical Library
  JOURNAL ANNOUNCEMENT: IAA9110
  Systolic Kalman filter (SKF) designs based on a **triangular** array
(triarray) configuration are presented. A least squares formulation, which
is an expanded **matrix** **representation** of the state space iteration, is
adopted to develop an efficient iterative QR triangularization and
consecutive data prewhitening formulations. This formulation has advantages
in both numerical accuracy and processor utilization efficiency. Moreover,
it leads naturally to pipelined architectures such as systolic or wavefront
arrays. For an n state and m measurement dynamic system, the SKF triarray
design uses n(n + 3)/2 processors and requires only 4n + m timesteps to
complete one iteration of prewhitened Kalman filtering system. This means a
speedup factor of approximately n-squared/4 when compared with a sequential
processor. Also proposed for the colored noise case are data prewhitening
triarrays which offer compatible speedup **performance** for the
preprocessing stage. Based on a comparison of several competing
alternatives, the proposed **array** **processor** may be considered a most
efficient systolic or wavefront design for Kalman filtering. (I.E.)
    SOURCE OF ABSTRACT/SUBFILE: AIAA

 11/7/8   (Item 1 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)
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04934662   E.I. No: EIP98024058238
  Title: **Efficient parallel computation of unstructured finite element
reacting flow solutions**
  Author: Shadid, John; Hutchinson, Scott; Hennigan, Gary; Moffat, Harry;
Devine, Karen; Salinger, A.G.
   Corporate Source: Sandia Natl Lab, Albuquerque, NM, USA
   Source: Parallel Computing v 23 n 9 Sep 1997. p 1307-1325
   Publication Year: 1997
   CODEN: PACOEJ   ISSN: 0167-8191
   Language: English
   Document Type: JA; (Journal Article)   Treatment: A; (Applications); T;
(Theoretical)
   Journal Announcement: 9804W2
   Abstract: A parallel unstructured finite element (FE) reacting flow
solver designed for message passing MIMD computers is described. This
implementation employs automated partitioning algorithms for **load**
balancing unstructured grids, a distributed sparse **matrix** **representation**
 of the global FE equations, and parallel Krylov subspace iterative

solvers. In this paper, a number of issues related to the efficient
implementation of parallel unstructured mesh applications are presented.
These issues include the differences between structured and unstructured
mesh parallel applications, major communication kernels for unstructured
Krylov iterative solvers, automatic mesh partitioning algorithms, and the
influence of mesh partitioning metrics and single-**node** CPU **performance**
on parallel **performance** . Results are presented for example FE heat
transfer, fluid flow and full reacting flow applications on a 1024
processor nCUBE 2 **hypercube** and a 1904 processor Intel Paragon. Results
indicate that very high computational rates and high scaled efficiencies
can be achieved for large problems despite the use of sparse matrix data
structures and the required unstructured data communication. (Author
abstract) 25 Refs.

11/7/9   (Item 2 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)
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04905323   E.I. No: EIP98014000145
 Title: **Optimized geometry compression for real-time rendering**
   Author: Chow, Mike M.
   Corporate Source: Massachusetts Inst of Technology, Cambridge, MA, USA
   Conference Title: Proceedings of the 1997 IEEE Visualization Conference
   Conference   Location: Phoenix,   AZ,   USA   Conference   Date:
19971019-19971024
   Sponsor: IEEE
   E.I. Conference No.: 47571
   Source: Proceedings of the IEEE Visualization Conference 1997. IEEE Comp
Soc, Los Alamitos, CA, USA,97CB36155. p 347-354
   Publication Year: 1997
   CODEN: 001061
   Language: English
   Document Type: CA; (Conference Article)   Treatment: T; (Theoretical)
   Journal Announcement: 9803W1
   Abstract: Most of existing **visualization** applications use **3D** geometry
as their basic rendering primitive. As users demand more complex datasets,
the memory requirements for retrieving and storing large 3D models are
becoming excessive. In addition, the current 3D rendering hardware is
facing a large memory bus bandwidth **bottleneck** at the **processor** to
graphics **pipeline** interface. Rendering 1 million **triangles** with 24
bytes per **triangle** at 30Hz requires as much as 720 MB/sec memory bus
bandwidth. This transfer rate is well beyond the current low-cost graphics
systems. A solution is to compress the static 3D geometry as an off-line
pre-process. Then, only the compressed geometry needs to be stored in main
memory and sent down to the graphics pipeline for real-time decompression
and rendering. We present several new techniques for compression of 3D
geometry that produce 2 to 3 times better compression ratios than existing
methods. We first introduce several algorithms for the efficient encoding
of the original geometry as generalized **triangle** meshes. This encoding
allows most of the mesh **vertices** to be reused when forming new **triangles**
. Our second contribution allows various parts of a geometric model to be
compressed with different precision depending on the level of details
present. Together, our meshifying algorithms and the variable compression
method achieve compression ratios of 30 and 37 to one over ASCII encoded
formats and 10 and 15 to one over binary encoded **triangle** strips. Our
experimental results show a dramatically lowered memory bandwidth required
for real-time **visualization** of complex datasets. (Author abstract) 11
Refs.

11/7/10   (Item 3 from file: 8)

04700089   E.I. No: EIP97053662585
 Title: **Data dependent optimizations for permutation volume rendering**
   Author: Wittenbrink, Craig M.; Kim, Kwansik
   Corporate Source: Hewlett-Packard Lab, Palo Alto, CA, USA
   Source: HP Laboratories Technical Report n 97-59 Apr 1997. p 1-19
   Publication Year: 1997
   CODEN: HLTREY
   Language: English
   Document Type: RR; (Report Review)   Treatment: T; (Theoretical); X;
(Experimental)
   Journal Announcement: 9707W3

   Abstract: Volume rendering is a class of algorithms for creating images
from volume sampled data sets without computing intermediate surface
representations. Because of the inherent O(N**3) run time, numerous
approximations are used to provide interactivity. One approach for high
performance is parallelization on general purpose computers. We have
developed a highly efficient, high fidelity approach that is called
permutation warping. Permutation warping may use any one pass filter
kernel, an example of which is trilinear reconstruction. Lacroute et al.'s
shear warp uses a bilinear multipass filter, for fewer operations, but an
inferior transfer function. This paper discusses experiments in improving
permutation warping using data dependent optimizations. We use a linear
octree on each processor to encode coherent and empty regions efficiently,
and to provide a means for adaptive resampling. Static **load** balancing is
also used to redistribute **nodes** from processor's octtree to achieve
higher efficiencies. **Performance** timings from a 4096 processor MasPar
MP-2 implementation show a 3 to 5 times speedup over brute force
permutation warping, depending upon the dataset. Actual **performance** is 3
to 4 frames/second on 128 multiplied by 128 multiplied by 128 volumes.
Because of the scalability of permutation warping, **performance** of 12-16
frames/second is expected on a 16,384 processor machine. It is expected
that implementation on more current SIMD or MIMD architectures would
provide 30-60 frames/second on larger volumes. (Author abstract) 31 Refs.

 11/7/11   (Item 4 from file: 8)

04549403   E.I. No: EIP96110405284
 Title: **Parallel spectral model for atmospheric transport processes**
   Author: Kindler, Thomas; Schwan, Karsten; Silva, Dilma; Trauner, Mary;
Alyea, Fred
   Corporate Source: Georgia Inst of Technology, Atlanta, GA, USA
   Source: Concurrency Practice and Experience v 8 n 9 Nov 1996. p 639-666
   Publication Year: 1996
   CODEN: CPEXEI   ISSN: 1040-3108
   Language: English
   Document Type: JA; (Journal Article)   Treatment: T; (Theoretical)
   Journal Announcement: 9701W1

   Abstract: The paper describes a parallel implementation of a grand
challenge problem: global atmospheric modeling. The novel contributions of
our work include (1) a detailed investigation of opportunities for
parallelism in atmospheric global modeling based on spectral solution
methods, (2) the experimental evaluation of overheads arising from **load**
imbalances and data movement for alternative parallelization methods, and
(3) the development of a parallel code that can be monitored and steered
interactively based on output data visualizations and animations of program
functionality or **performance** . Code parallelization takes advantage of the

relative independence of computations at different levels in the earth's
atmosphere, resulting in parallelism of up to 40 processors, each
independently performing computations for different atmospheric levels and
requiring few communications between different levels across model time
steps. Next, additional parallelism is attained within each level by taking
advantage of the natural parallelism offered by the spectral computations
being performed (e.g. taking advantage of independently computable terms in
equations). **Performance** measurements are performed on a 64-**node** KSR2
supercomputer. However, the parallel code has been ported to several shared
memory parallel machines, including SGI multiprocessors, and has also been
ported to distributed memory platforms like the IBM SP-2. (Author abstract)
38 Refs.

11/7/12   (Item 5 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)
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04538262   E.I. No: EIP96100382886
   Title: **RIVA: A versatile parallel rendering system for interactive
scientific** visualization
   Author: Li, P. Peggy; Duquette, William H.; Curkendall, David W.
   Corporate Source: Jet Propulsion Lab, Pasadena, CA, USA
   Source: IEEE Transactions on Visualization and Computer Graphics v 2 n 3
Sep 1996. p 186-201
   Publication Year: 1996
   CODEN: ITVGEA
   Language: English
   Document Type: JA; (Journal Article)   Treatment: G; (General Review)
   Journal Announcement: 9612W4
   Abstract: JPL's Remote Interactive **Visualization** and Analysis System
(RIVA) is described in detail. The RIVA system integrates workstation
graphics, massively parallel computing technology, and gigabit
communication networks to provide a flexible interactive environment for
scientific data perusal, analysis, and **visualization** . RIVA's kernel is a
highly scalable parallel perspective renderer tailored especially for the
demands of large datasets beyond the sensible reach of workstations. Early
experience with using RIVA to interactively explore and process
multivariate, multiresolution datasets is reported; several examples using
data from a variety of remote sensing instruments are discussed in detail
and the results shown. Particular attention is placed on describing the
algorithmic details of RIVA's parallel renderer kernel, with emphasis on
the key aspects of achieving the algorithm's overall scalability. The paper
summarizes the **performance** achieved for machine sizes up to more than 500
 nodes and for initial input image/terrain bases in the 2 Gbyte range.
(Author abstract) 14 Refs.

11/7/13   (Item 6 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)
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04528219   E.I. No: EIP96103361890
   Title: **Architectural optimizations for a floating point
multiply-accumulate unit in a graphics pipeline**
   Author: Acken, K.P.; Irwin, M.J.; Owens, R.M.; Garga, A.K.
   Corporate Source: The Pennsylvania State Univ, University Park, PA, USA
   Conference Title: Proceedings of the 1996 International Conference on
Application-Specific Systems, Architectures and Processors
   Conference Location: Chicago, IL, USA Conference Date:
19960819-19960821
   Sponsor: IEEE

E.I. Conference No.: 45391
  Source: International   Conference   on   Application-Specific   Systems,
Architectures and Processors, Proceedings 1996. IEEE, Piscataway, NJ, USA.
p 65-71
  Publication Year: 1996
  CODEN: 002451
  Language: English
  Document Type: CA; (Conference Article)   Treatment: A; (Applications); T
; (Theoretical)
  Journal Announcement: 9612W2
  Abstract: Scientific **visualization** and virtual reality have pushed
three -dimensional graphics engines to their limits for updating scenes
in real-time. One **bottleneck** of graphic systems is the transformation of
an object's **vertices** into normalized space based on an evaluated
transformation stack. This operation is often done in floating point,
requiring a fast floating point multiply-accumulate unit. This paper
presents architectural optimizations to a graphics pipeline floating point
multiply-accumulate unit by using block floating point and parallelism to
bypass or merge trivial operations in the matrix multiplications. (Author
abstract) 9 Refs.

  11/7/14   (Item 7 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)
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04313346   E.I. No: EIP95122957144
  Title: **Remote interactive** visualization **and analysis (RIVA) using
parallel supercomputers**
  Author: Li, P. Peggy; Duquette, William H.; Curkendall, David W.
  Corporate Source: Jet Propulsion Lab, Pasadena, CA, USA
  Conference Title: Proceedings of the 1995 Parallel Rendering Symposium
  Conference   Location: Atlanta,   GA,   USA   Conference   Date:
19951030-19951031
  Sponsor: IEEE; ACM/SIGGRAPH
  E.I. Conference No.: 44067
  Source: Proc 1995 Parall Rendering Symp 1995. ACM. p 71-78
  Publication Year: 1995
  Language: English
  Document Type: CA; (Conference Article)   Treatment: A; (Applications)
  Journal Announcement: 9602W3
  Abstract: JPL's Remote Interactive **Visualization** and Analysis System
(RIVA) is described in detail. RIVA's kernel is a highly scalable
perspective renderer tailored especially for the demands of large datasets
beyond the sensible reach of workstations. The algorithmic details of this
renderer are described, particularly the aspects key to achieving the
algorithm's overall scalability. The paper summarizes the **performance**
achieved for machine sizes up to more than 500 **nodes** and for initial
input image/terrain bases of up to a gigabyte. The RIVA system integrates
workstation graphics, massively parallel computing technology, and gigabit
communication networks to provide a flexible interactive environment for
scientific data perusal, analysis and **visualization** . Early experience
with using RIVA to interactively explore multivariate datasets is reported
and some example results given. (Author abstract) 12 Refs.

  11/7/15   (Item 8 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)
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04313344   E.I. No: EIP95122957142
  Title: **Image composition methods for sort-last polygon rendering on 2-D**

mesh architectures
   Author: Lee, Tong-Yee; Raghavendra, C.S.; Nicholas, J.N.
   Corporate Source: Washington State Univ, Pullman, WA, USA
   Conference Title: Proceedings of the 1995 Parallel Rendering Symposium
   Conference   Location: Atlanta,   GA,   USA   Conference   Date:
19951030-19951031
   Sponsor: IEEE; ACM/SIGGRAPH
   E.I. Conference No.: 44067
   Source: Proc 1995 Parall Rendering Symp 1995. ACM. p 55-62
   Publication Year: 1995
   Language: English
   Document Type: CA; (Conference Article)   Treatment: A; (Applications); T
; (Theoretical)
   Journal Announcement: 9602W3

   Abstract: In this paper, a new sort-last parallel polygon rendering
implementation is given for 2-D mesh message-passing architectures such as
the Intel Delta and Paragon. Our implementation provides a very fast
rendering rate for extremely large sets of polygons, a requirement of
scientific **visualization** , CAD/CAM, and many other applications. We
implement and evaluate our scheme on the Intel Delta parallel computer at
Caltech. Using 512 processors to render Eric Haines's SPD standard scenes,
our scheme achieves a rendering rate of 2.8 - 4.0 million **triangles**
/second. (Author abstract) 21 Refs.

   11/7/16   (Item 9 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)

04264406   E.I. No: EIP95102886308
   Title: **Architecture-independent locality-improving transformations of
computational graphs embedded in k-dimensions**
   Author: Ou, Chao-Wei; Gunwani, Manoj; Ranka, Sanjay
   Corporate Source: Syracuse Univ, Syracuse, NY, USA
   Conference Title: Proceedings of the 1995 Conference on Supercomputing
   Conference   Location: Barcelona,   Spain   Conference   Date:
19950703-19950707
   Sponsor: ACM; SIGARCH
   E.I. Conference No.: 43707
   Source: Proceedings of the International Conference on Supercomputing
1995. ACM, New York, NY, USA. p 289-298
   Publication Year: 1995
   CODEN: 002151
   Language: English
   Document Type: CA; (Conference Article)   Treatment: A; (Applications); T
; (Theoretical)
   Journal Announcement: 9512W1

   Abstract: A large number of data-parallel applications can be represented
as computational graphs from the perspective of parallel computing. The
nodes of these graphs represent tasks that can be executed concurrently,
while the edges represent the interactions between them. Further, the
computational graphs derived from many applications are such that the
vertices correspond to multi-dimensional coordinates, and the interaction
between computations is limited to **vertices** that are physically
proximate. In this paper we show that graphs with these properties can be
transformed into simple architecture-independent representations that
encapsulate the locality in these **graphs** . This **representation** allows a
fast mapping of the computational graph onto the underlying architecture at
the **time** of **execution** . This is necessary for environments where
available computational **resources** can be determined only at the **time** of
 execution or that change during execution. (Author abstract) 32 Refs.

11/7/17   (Item 10 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)

04142417   E.I. No: EIP95042673939
 Title: Recursive spectral algorithms for automatic domain partitioning in parallel finite element analysis
   Author: Hsieh, Shang-Hsien; Paulino, Glaucio H.; Abel, John F.
   Corporate Source: Purdue Univ, West Lafayette, IN, USA
   Source: Computer Methods in Applied Mechanics and Engineering v 121 n 1-4 Mar 1995. p 137-162
   Publication Year: 1995
   CODEN: CMMECC   ISSN: 0045-7825
   Language: English
   Document Type: JA; (Journal Article)   Treatment: T; (Theoretical)
   Journal Announcement: 9506W3
   Abstract: Recently, several domain partitioning algorithms have been proposed to effect **load** -balancing among **processors** in **parallel** finite element analysis. The recursive spectral bisection (RSB) algorithm left bracket 1 right bracket has been shown to be effective. However, the bisection nature of the RSB results in partitions of an integer power of two, which is too restrictive for computing environments consisting of an arbitrary number of processors. This paper presents two recursive spectral partitioning algorithms, both of which generalize the RSB algorithm for an arbitrary number of partitions. These algorithms are based on a graph partitioning approach which includes spectral techniques and **graph representation** of finite element meshes. The 'algebraic connectivity vector' is introduced as a parameter to assess the quality of the partitioning results. Both **node** -based and element-based partitioning strategies are discussed. The spectral algorithms are also evaluated and compared for coarse-grained partitioning using different types of structures modelled by 1-D, 2-D and 3-D finite elements. (Author abstract) 28 Refs.

11/7/18   (Item 11 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)

04094636   E.I. No: EIP95032610560
 Title: Ductile failure analyses on massively parallel computers
   Author: Mathur, K.K.; Needleman, A.; Tvergaard, V.
   Corporate Source: Thinking Machines Corp, Cambridge, MA, USA
   Source: Computer Methods in Applied Mechanics and Engineering v 119 n 3-4 Dec 1994. p 283-309
   Publication Year: 1994
   CODEN: CMMECC   ISSN: 0045-7825
   Language: English
   Document Type: JA; (Journal Article)   Treatment: A; (Applications); T; (Theoretical)
   Journal Announcement: 9505W1
   Abstract: Full three-dimensional analyses of ductile failure are carried out for tensile test specimens under dynamic loading, using a data parallel implementation of a ductile porous material model in a transient 3D finite element program. The elastic-viscoplastic material model accounts for ductile failure by the nucleation, growth and coalescence of micro-voids. Most of the results are obtained using 20 **node** isoparametric brick elements and reduced (2 multiplied by 2 multiplied by 2) quadrature. The capabilities of the model are checked by a number of simulations for one layer of elements subject to overall plane strain conditions, compared to plane strain predictions. Comparisons are made with results using other

orders of interpolation and other quadrature rules. It is shown that the high order **3D** elements give a good **representation** of shear localization. For a uniaxial tensile test specimen with a square cross-section, full three-dimensional computations are carried out with meshes consisting of many brick elements in each coordinate direction, and these analyses are used to study the final failure mode in the neck region. The scalability of the parallel implementation is verified and the **performance** with the porous plastic constitutive relation is compared with that obtained using a standard isotropic hardening model. (Author abstract) 36 Refs.

11/7/19   (Item 12 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)
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04082723   E.I. No: EIP95022584413
 Title: **Distributed, parallel, interactive volume rendering package**
  Author: Rowlan, John S.; Lent, G. Edward; Gokhale, Nihar; Bradshaw, Shannon
  Corporate Source: Argonne Natl Lab, Argonne, IL, USA
  Conference Title: Proceedings of the 1994 IEEE Visualization Conference
  Conference   Location: Washington,   DC,   USA   Conference   Date: 19941017-19941021
  Sponsor: IEEE; ACM; SIGGRAPH
  E.I. Conference No.: 42510
  Source: Proceedings   Visualization   1994.   IEEE,   Los   Alamitos,   CA, USA,94CH35707. p 21-30
  Publication Year: 1994
  CODEN: 001061   ISSN: 1070-2385
  Language: English
  Document Type: CA; (Conference Article)   Treatment: A; (Applications); T ; (Theoretical)
  Journal Announcement: 9504W4
  Abstract: This paper presents a parallel ray-casting volume rendering algorithm and its implementation on the massively parallel IBM SP-1 computer using the Chameleon message passing library. Though this algorithm takes advantage of many of the unique features of the SP-1 (e.g. high-speed switch, large memory per **node** , high-speed disk array, HIPPI display, et al), the use of Chameleon allows the code to be executed on any collection of workstations. The algorithm is image-ordered and distributes the data and the computational **load** to individual processors. After the volume data is distributed, all processors then perform local raytracing of their respective subvolumes concurrently. No interprocess communication takes place during the ray tracing process. After a subimage is generated by each processor, the final image is obtained by composing subimages between all the processors. The program itself is implemented as an interactive process through a GUI residing on a graphics workstation which is coupled to the parallel rendering algorithm via sockets. The paper highlights the Chameleon implementation, the GUI, some optimization improvements, static **load** balancing, and direct parallel display to a HIPPI framebuffer. (Author abstract) 11 Refs.

11/7/20   (Item 13 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)
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04038520   E.I. No: EIP95012507220
 Title: **Automatic clustering algorithm using factorisation tree for parallel power system simulation**
  Author: Bialek, J.; Grey, D.J.

Corporate Source: Univ of Durham, Durham, Engl
Conference   Title: Proceedings of the 7th Mediterranean Electrotechnical
Conference - MELECON. Part 3 (of 3)
Conference Location: Antalya, TURKEY   Conference Date: 19940412-19940414
Sponsor: IEEE;   Middle   East   Technical   University; Bilkent University;
Chamber of Electrical Engineers of Turkey
E.I. Conference No.: 42119
Source: Mediterranean Electrotechnical Conference - MELECON 3 (of 3 1994.
IEEE, Piscataway, NJ, USA, 94CH3388-6. p 980-983
Publication Year: 1994
CODEN: 001676
Language: English
Document Type: CA; (Conference Article)   Treatment: A; (Applications)
Journal Announcement: 9503W3

Abstract: Parallel simulation of power systems requires the system to be
partitioned into subnetworks which are processed on individual processors.
Maximum computational efficiency is achieved when the network is split such
that each processors has an equal computational **load** . This paper proposes
an automatic method of network partitioning which gives well balanced
network splits, based upon an analysis of the factorisation tree for the
system. The method also predicts the expected parallel speed-up for the
split and allows the **visualisation** of large networks. A modified Minimum
Degree Minimum Length **node** ordering algorithm is also presented which
gives well balanced factorisation trees. (Author abstract) 13 Refs.

11/7/21   (Item 14 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)
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04024659   E.I. No: EIP94122499470
 Title: **Multimedia** performance **behavior of the GigaView** parallel **image**
 server
 Author: Gennart, Benoit A.; Hersch, Roger D.
 Corporate   Source: Ecole   Polytechnique   Federale de Lausanne, Lausanne,
Switz
 Conference   Title: Proceedings of the 1994 13th Symposium on Mass Storage
Systems
 Conference Location: Annecy, Fr   Conference Date: 19940612-19940616
 Sponsor: IEEE
 E.I. Conference No.: 21462
 Source: Digest   of Papers - IEEE Symposium on Mass Storage Systems 1994.
IEEE, Piscataway, NJ, USA, 94CH3457-9. p 90-98
 Publication Year: 1994
 CODEN: DPISDX   ISSN: 1051-9173
 Language: English
 Document Type: CA; (Conference Article)   Treatment: G; (General Review)
 Journal Announcement: 9502W4

Abstract: Multimedia interfaces increase the need for large image
databases, supporting the capability of storing and fetching streams of
data with strict synchronicity and isochronicity requirements. In order to
fulfill these requirements, the GigaView **parallel** image **server**
architecture relies on arrays of intelligent disk **nodes** , with each disk
node being composed of one processor and one disk. This paper analyzes,
through simulation, the real-time behavior of the GigaView in terms of
delay and delay jitter. For a high-end GigaView architecture, consisting of
16 disks and T9000 transputers, we evaluate stream frame access times under
various parameters, such as **load** factors, frame size, stream **throughput**
, and synchronicity requirements. (Author abstract) 8 Refs.

11/7/22   (Item 15 from file: 8)

03987402   E.I. No: EIP94112421822
   Title: **Distributed**   **sparse**   **Gaussian**   **elimination**   and   **orthogonal**
factorization
   Author: Raghavan, Padma
   Corporate Source: Univ of Illinois, Urbana, IL, USA
   Conference Title: Proceedings of the Scalable High-Performance Computing
Conference
   Conference   Location: Knoxville,   TN,   USA   Conference   Date:
19940523-19940525
   Sponsor: IEEE Computer Society
   E.I. Conference No.: 21190
   Source: Proceedings of the Scalable High-Performance Computing Conference
1994. IEEE, Los Alamitos, CA, USA. p 607-614
   Publication Year: 1994
   CODEN: 85OZA6
   Language: English
   Document Type: CA; (Conference Article)   Treatment: G; (General Review);
T; (Theoretical)
   Journal Announcement: 9501W1
   Abstract: We consider the solution of a linear system Ax equals b on a
distributed memory machine when the matrix A has full rank and is large,
sparse and nonsymmetric. We use our parallel Cartesian Nested Dissection
algorithm to compute a fill-reducing ordering of A using a compact
representation of the column intersection **graph** . We develop and
implement simple algorithms that use the resulting separator tree to
estimate the structure of the factor and to distribute data and perform
multifrontal numeric computations. When the matrix is nonsymmetric but
square, the numeric computations involve Gaussian elimination with row
pivoting; when the matrix is overdetermined, row-oriented Householder
transforms are applied to compute the **triangular** factor of an orthogonal
factorization. Our main contribution is the formulation of a fully
parallel, unified approach to solving nonsymmetric sparse systems using
either Gaussian elimination or orthogonal factorization and empirical
results to demonstrate that the approach is effective both in reducing fill
and achieving good parallel **performance** on an Intel iPSC/860. (Author
abstract) 20 Refs.

   11/7/23   (Item 16 from file: 8)

03987356   E.I. No: EIP94112421776
   Title: Load **balancing** **of** **parallel** **volume** **rendering** **with** **scattered**
decomposition
   Author: Karia, Raju J.
   Corporate Source: Australian Natl Univ, Canberra, Aust
   Conference Title: Proceedings of the Scalable High-Performance Computing
Conference
   Conference   Location: Knoxville,   TN,   USA   Conference   Date:
19940523-19940525
   Sponsor: IEEE Computer Society
   E.I. Conference No.: 21190
   Source: Proceedings of the Scalable High-Performance Computing Conference
1994. IEEE, Los Alamitos, CA, USA. p 252-258
   Publication Year: 1994
   CODEN: 85OZA6
   Language: English
   Document Type: CA; (Conference Article)   Treatment: G; (General Review)

Journal Announcement: 9501W1

Abstract: A scheme for the **visualization** of large data volumes using volume rendering on a distributed memory MIMD system is described. The data to be rendered is decomposed into subvolumes to reside in the local memories of the system's **nodes** . A partial image of the local data is generated at each **node** by ray tracing, and is then composited with partial images on other **nodes** in the correct order to generate the complete image. Subvolumes whose voxels are classified as being mapped to zero opacity are not rendered, giving rise to an imbalance of work amongst **nodes** . Scattered decomposition is used for **load** balancing, which on one hand, creates additional overheads in compositing and communication, but on the other, provides an improvement in **throughput** that is dependent on the characteristics of the data. Experimental results for a typical data set rendered on a 1024-**node** Fujitsu AP1000 are reported. (Author abstract) 13 Refs.

11/7/24   (Item 17 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)

03954591   E.I. No: EIP94101424153
 Title: **Gigabit network applications at Los Alamos National Laboratory**
   Author: Morrison, John
   Corporate Source: Los Alamos Natl Lab, Los Alamos, NM, USA
   Conference Title: Proceedings of the 1994 Optical Fiber Communication Conference
   Conference Location: San Jose, CA, USA Conference Date: 19940220-19940225
   Sponsor: Lasers and Electro-Optics Society of the IEEE; Optical Society of America; Communications Society of the IEEE
   E.I. Conference No.: 20322
   Source: Conference on Optical Fiber Communication, Technical Digest Series v 4 1994. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA. p 64-65
   Publication Year: 1994
   CODEN: COFCEL   ISBN: 1-55752-330-4
   Language: English
   Document Type: CA; (Conference Article)   Treatment: A; (Applications); G ; (General Review); T; (Theoretical)
   Journal Announcement: 9411W3
   Abstract: The Department of Energy High **Performance** Computing Research Center (HPCRC) at Los Alamos National Laboratory, one of two DOE-sponsored centers, employs gigabit-per-second networks to interconnect high-**performance** computing systems, storage systems, and **visualization** systems to create an integrated computational environment serving the needs of Grand Challenge-scale scientific applications. A diagram of this computational environment is shown in Fig. 1. The primary computational **resource** , a Thinking Machines Corp. 1024-**node** CM-5 with 32 Gbyte of memory and four 800-Mbit/s high-**performance** parallel-interface (HIPPI) channels is used by several applications to model complex physical processes. One of these applications, a state-of-the-art global ocean model, generates several hundred gigabytes of data during a long simulation. Global ocean models must run for several decades of simulated time because of the physical properties of the ocean. These calculations typically require hundreds of hours on the world's fastest supercomputers and consequently do not generate data at gigabit-per-second rates. The results of these calculations is a multigigabyte file containing the time- and space-dependent values of various physical properties, such as temperature and velocity. These results are typically visualized on a high-resolution frame buffer driven at gigabit-per-second rates. A fast disk system is used to store the data and to stream it to the frame buffer.

Moving data from mass storage to a frame buffer at near gigabit-per-second rates motivated the design of a new file-system architecture. This architecture eliminates the traditional mainframe **bottleneck** between the disk storage devices and the network by attaching the storage devices directly to the network. We have achieved rates of 60 Mbit/s from a RAID disk array to a frame buffer system attached to a HIPPI-based network. Gigabit-per-second networks are permitting new approaches to file system architectures and **visualization** systems. These high-**performance** file systems and **visualization** systems, coupled with supercomputers, provide powerful tools in the quest for solutions to Grand Challenge-scale problems. (Author abstract)

11/7/25   (Item 18 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)
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03802137   E.I. No: EIP94021213879
 Title: **Efficient parallel sibling finding for quadtree data structure**
   Author: Doctor, Dipak Pravin; Sudborough, Hal
   Corporate Source: Univ of Texas at Dallas, Richardson, TX, USA
   Conference Title: Proceedings of the 5th IEEE Symposium on Parallel and Distributed Processing
   Conference Location: Dallas, TX, USA   Conference Date: 19931201-19931204
   Sponsor: IEEE Computer Society
   E.I. Conference No.: 19912
   Source: Proceedings of the 5th IEEE Symposium on Parallel and Distributed Processing Proc 5 IEEE Symp Parallel Distrib Proc 1993. Publ by IEEE, Computer Society Press, Los Alamitos, CA, USA. p 141-148
   Publication Year: 1993
   ISBN: 0-8186-4222-X
   Language: English
   Document Type: CA; (Conference Article)   Treatment: G; (General Review); T; (Theoretical)
   Journal Announcement: 9404W1
   Abstract: This paper presents efficient parallel (**hypercube** and EREW-PRAM) algorithms for building pointer-based and linear quadtrees from boundary/chain code **image   representation** . For the input boundary code of length O(b) and the height O(h) of the output quadtree, our EREW-PRAM algorithm takes O(h plus logb) time and O(b) processors for quadtree building from boundary code; this improves upon a previously published CREW-PRAM algorithm requiring O(h*logb) time and O(b) processors. For the same task, our **hypercube** algorithm takes O(h*logb) time and O(b) processors; which also improves upon a previously published **hypercube** algorithm requiring O(logb(h plus log**2logb)) time and O(b) processors. The algorithms, presented here, use a direct and simple sibling finding technique for quadtrees; our technique exploits regularity in quadtree data structure, and it is applicable to any k-ary tree for which some (arbitrary) ordering exists among child **nodes** of a parent **node** . (Author abstract) 17 Refs.

11/7/26   (Item 19 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)
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03685051   E.I. No: EIP93040763679
   Title: **Parallel   rendering of volumetric data set on distributed-memory architectures**
   Author: Montani, C.; Perego, R.; Scopigno, R.
   Corporate Source: Instituto CNUCE, Pisa, Italy
   Source: Concurrency Practice and Experience v 5 n 2 Apr 1993. p 153-167

17 May 10, 2000 10:56

Publication Year: 1993
CODEN: CPEXEI   ISSN: 1040-3108
Language: English
Document Type: JA; (Journal Article)   Treatment: T; (Theoretical); A;
(Applications)
Journal Announcement: 9310W2

Abstract: A solution is proposed to the problem of interactive
visualization and rendering of volume data. Designed for parallel
distributed memory (MIMD) architectures, the volume rendering system is
based on the ray tracing (RT) **visualization** technique, the Sticks
representation scheme (a data structure exploiting data coherence for the
compression of classified data sets), the use of a slice-partitioning
technique for the distribution of the data between the processing **nodes**
and the consequent ray-data-flow parallelizing strategy. The system has
been implemented on two different architectures: an inmos Transputer
network and a **hypercube** nCUBE 6400 architecture. The high number of
processors of this latter machine is allowed us to exploit a second level
of parallelism (parallelism on image space, or parallelism on pixels) in
order to arrive at a higher degree of scalability. In both proposals, the
similarities between the chosen data-partitioning strategy, the
communications pattern of the **visualization** processes and the topology of
the physical system architecture represent the key points and provide
improved software design and efficiency. Moreover, the partitioning
strategy used and the network interconnection topology reduce the
communications overhead and allow for an efficient implementation of a
static **load** -balancing technique based on the prerendering of a low
resolution image. Details of the practical issues involved in the
parallelization process of volumetric RT, commonly encountered problems
(i.e. termination and deadlock prevention) and the sw migration process
between different architectures are discussed. (Author abstract) 21 Refs.

11/7/27   (Item 20 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)
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03603258   E.I. Monthly No: EIM9305-024749
   Title: **DELTA-T: a user-transparent software-monitoring tool for**
multi-transputer systems.
   Author: Maehle, Erik; Obeloer, Wolfgang
   Corporate Source: Universitat-GH-Paderborn, Paderborn, Germany
   Conference   Title: 18th EUROMICRO Symposium on Microprocessing and
Microprogramming - EUROMICRO 92
   Conference Location: Paris, Fr   Conference Date: 19920914
   E.I. Conference No.: 17255
   Source: Microprocessing and Microprogramming v 35 n 1-5 Sep 1992. p
245-252
   Publication Year: 1992
   CODEN: MMICDT   ISSN: 0165-6074
   Language: English
   Document Type: JA; (Journal Article)   Treatment: X; (Experimental); A;
(Applications)
   Journal Announcement: 9305
   Abstract: Monitoring tools are important parts of future programming
environments for parallel computers. In this paper the software monitor
DELTA-T is presented which has been developed for **performance** monitoring
of (standard) multi-transputer systems at the University of Paderborn.
Instrumentation is implemented by 'spy'-processes which are inserted into
the target system either to observe it at the **node** or at the process
level. Measurement traces generated by these spies are buffered locally in
the **node** memories. A global system view is achieved by time-stamping the
recorded events with a globally valid system time. Evaluation is carried

out offline on a host workstation either with an animation tool or an
interactive **graphical   visualization** tool. (Author abstract) 14 Refs.

11/7/28   (Item 21 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)
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03562656   E.I. Monthly No: EIM9302-011085
 Title: A performance **monitor for the MSPARC multicomputer.**
  Author: Harden, J.; Reese, D.; To, F.; Linder, D.; Borchert, C.; Jones,
G.
  Conference Title: Proceedings of the IEEE SOUTHEASTCON '92
  Conference Location: Birmingham, AL, USA   Conference Date: 19920412
  Sponsor: IEEE Alabama Section; IEEE Region 3
  E.I. Conference No.: 17598
  Source: Conference Proceedings – IEEE SOUTHEASTCON v 2. Publ by IEEE,
IEEE Service Center, Piscataway, NJ, USA (IEEE cat n 92CH3094-0). p 724-729
  Publication Year: 1992
  CODEN: CPISDM   ISSN: 0734-7502   ISBN: 0-7803-0494-2
  Language: English
  Document Type: PA; (Conference Paper)   Treatment: T; (Theoretical); A;
(Applications)
  Journal Announcement: 9302
  Abstract: A hybrid **performance** monitor developed for MSPARC, a
mesh-connected, message-passing multicomputer, is described. The
development of the hybrid **performance** monitor was a cross-disciplinary
enterprise requiring custom hardware and a range of software support
including monitor code, driver interfaces, probe history acquisition and
processing, graphical display, and application probe injection.
Programmable hardware was designed to unobtrusively collect events on each
node and maintain their accurate chronological order. This distributed
collection system was coupled by its independent network to a central
monitor where data selection and presentation techniques played an
important role in the **visualization** of the parallel system's execution.
13 Refs.

11/7/29   (Item 22 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)
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03481275   E.I. Monthly No: EI9209110643
 Title: Using visualization **tools to understand** concurrency.
  Author: Zernik, Dror; Snir, Marc; Malki, Dalia
  Corporate Source: Dept of Electr Eng, Technion, Haifa, Israel
  Source: IEEE Software v 9 n 3 May 1992 p 87-92
  Publication Year: 1992
  CODEN: IESOEG   ISSN: 0740-7459
  Language: English
  Document Type: JA; (Journal Article)   Treatment: A; (Applications); T;
(Theoretical); X; (Experimental)
  Journal Announcement: 9209
  Abstract: A **visualization** tool that provides an aggregate view of
execution through a graph of events called the causality graph, which is
suitable for systems with hundreds or thousands of processors,
coarse-grained parallelism, and for a language that makes communication and
synchronization explicit, is discussed. The methods for computing causality
graphs and stepping through an execution with causality graphs are
described. The properties of the abstraction algorithms and super **nodes** ,
the subgraphs in causality graphs, are also discussed. 4 Refs.

19 May 10, 2000 10:56

11/7/30 (Item 23 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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02981584 E.I. Monthly No: EI9011132047
 Title: **Implementing recurrent back-propagation on the Connection Machine**.
 Author: Deprit, Etienne
 Corporate Source: Naval Research Lab, Washington, DC, USA
 Source: Neural Networks v 2 n 4 1989 p 295-314
 Publication Year: 1989
 CODEN: NNETEB ISSN: 0893-6080
 Language: English
 Document Type: JA; (Journal Article) Treatment: T; (Theoretical); X;
(Experimental)
 Journal Announcement: 9011
Abstract: The recurrent back-propagation algorithm for neural networks
has been implemented on the Connection Machine, a massively **parallel
processor** . Two fundamentally different graph architectures underlying the
nets were tested: one based on arcs, the other on **nodes** . Confirming the
predominance of communication over computation, **performance** measurements
underscore the necessity to make connections the basic unit of
representation . Comparisons between these **graph** algorithms lead to
important conclusions concerning the parallel implementation of neural nets
in both software and hardware. (Author abstract) 16 Refs.

11/7/31 (Item 24 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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02788536 E.I. Monthly No: EI8909087140
 Title: **Parallel computer graphics simulation of the Lebanese Electric
Power System**.
 Author: Diab, Hassan; Yehia, Mounir; Abou-Hassan, Iman
 Corporate Source: American Univ, Beirut, Leban
 Source: IEEE Computer Applications in Power v 2 n 1 Jan 1989 p 38-42
 Publication Year: 1989
 CODEN: ICAPEH ISSN: 0895-0156
 Language: English
 Document Type: JA; (Journal Article) ,Treatment: A; (Applications)
 Journal Announcement: 8909
Abstract: A microcomputer software package that provides a computer
graphics simulation of electrical power systems in a **parallel -processing**
 configuration is described. It facilitates a user-friendly environment to
configure the electrical network so that hypothetical or actual substations
and transmission lines can be added or deleted to simulate any change in
the network's **performance** . The package runs in parallel with the **load**
-flow program and is used as a computer-aided design tool to provide a
graphical representation of the Lebanese electrical network, which is
composed of 127 **nodes** . The choice and implementation of the hierarchical
data structure used to store the network's model are examined.
Graphic-oriented reports, context-sensitive HELP, and online documentation
make the package a powerful tool that can analyze anything from a few buses
to an entire network. An important feature of the package is its fast
throughput of execution. 4 Refs.

11/7/32 (Item 25 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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02733551   E.I. Monthly No: EI8904032164
  **Title: General approach to mapping of parallel computations upon
multiprocessor architectures.**
  Author: Kim, S. J.; Browne, J. C.
  Corporate Source: Univ of Texas, Austin, TX, USA
  Conference Title: Proceedings of the 1988 International Conference on
Parallel Processing V 1, Architecture; v 2, Software; v 3, Algorithms and
Applications.
  Conference Location: University Park, PA, USA   Conference Date: 19880815
  Sponsor: Penn State Univ, University Park, PA, USA
  E.I. Conference No.: 11870
  Source: Proceedings of the International Conference on Parallel
Processing. Publ by Pennsylvania State University, University Park, PA,
USA. Available from IEEE Service Cent (cat n 88CH2625-2) Piscataway, NJ,
USA. p 1-8
  Publication Year: 1988
  CODEN: PCPADL   ISBN: 0-271-00654-4
  Language: English
  Document Type: PA; (Conference Paper)   Treatment: T; (Theoretical); E;
(Economic/Cost Data/Market Survey)
  Journal Announcement: 8904

  Abstract: A broadly applicable approach to mapping of parallel
computations on multiprocessors is described, and the related mapping
algorithms are briefly sketched. The approach begins with a **graph
representation** of a parallel computation and first generates a reduced
graph by merging **nodes** with high internode communication cost through
iterative use of a critical-path algorithm. This graph is then mapped to a
graphical representation of a multiprocessor architecture by the mapping
algorithms. These algorithms attempt to minimize the total **execution
time** , including both computation and communication times. The algorithms,
while they are heuristic rather than true optimal algorithms, are shown to
yield excellent results in example applications and have modest execution
costs. 23 Refs.

  11/7/33   (Item 1 from file: 35)
DIALOG(R)File 35:DISSERTATION ABSTRACTS ONLINE
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01631561 ORDER NO: AAD98-23300
**EXPLOITING MULTI-GRAINED PARALLELISM FOR MULTIPLE-INSTRUCTION-STREAM
ARCHITECTURES (PARALLELISM, REPRESENTATIONS, COMPILATION)**
  Author: NEWBURN, CHRISTOPHER JOHN
  Degree: PH.D.
  Year: **1997**
  Corporate Source/Institution: CARNEGIE-MELLON UNIVERSITY (0041)
  Adviser: JOHN PAUL SHEN
  Source: VOLUME 59/02-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
          PAGE 800. 178 PAGES

     Exploiting parallelism is an essential part of maximizing the
performance of an application on a parallel computer. Parallelism is
traditionally exploited at two granularities: individual operations are
executed in **parallel** within a **processor** to exploit instruction-level
parallelism and loop iterations or processes are executed in **parallel** on
different **processors** to exploit loop-level parallelism and process-level
parallelism.
     A new generation of architectures that execute multiple instruction
streams on a single chip has the potential of significantly reducing the
gap between communication costs within a processor and between processors.
This means that parallelism of multiple granularities can be exploited
between instruction streams by overlapping regions of code that range in

granularity from a small set of instructions to basic blocks, conditionals, loop iterations, loop nests, procedure calls, and collections of such constructs. This opens the way to exploiting more parallelism in a larger number of applications than has been feasible in the past. Furthermore, it creates a demand for compilation techniques which exploit multi-grained parallelism, that is, the overlap of program regions of different granularities.

This thesis studies the exploitation of multi-grained parallelism. It presents a program **representation** called the program dependence **graph** (PDG) and a **node** labeling scheme that supplements it. These representations have been specialized to expose multi-grained parallelism and facilitate its exploitation on a multiple-instruction-stream architecture. The thesis investigates novel compilation techniques for exploiting multi-grained parallelism and explores the impact of synchronization cost on **performance** . These techniques perform partitioning, scheduling and synchronization of a single application for a multiple-instruction-stream architecture. The partitioning techniques make global trade-offs to select the granularity of parallelism to exploit in each part of the program so as to minimize the overall latency for a target architecture. The thesis describes an implementation of these representations and techniques called Pedigree, which is the first post-pass, retargetable compiler to target multiple-instruction-stream architectures. The SDIO and some SPEC benchmarks have been compiled by Pedigree and used to demonstrate its ability to parallelize code. The best results for exploiting multi-grained parallelism come from overlapping parallelized loop nests, something which is new to this work.

11/7/34   (Item 2 from file: 35)
DIALOG(R)File 35:DISSERTATION ABSTRACTS ONLINE
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01556330 ORDER NO: AAD97-15692
POLYGON RENDERING FOR INTERACTIVE VISUALIZATION **ON MULTICOMPUTERS** (
PARALLEL   PROCESSING)
  Author: ELLSWORTH, DAVID ALLAN
  Degree: PH.D.
  Year: **1996**
  Corporate Source/Institution: THE UNIVERSITY OF NORTH CAROLINA AT CHAPEL
        HILL (0153)
  Adviser: HENRY FUCHS
  Source: VOLUME 57/12-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
        PAGE 7600. 370 PAGES

    This dissertation identifies a class of parallel polygon rendering algorithms suitable for interactive use on multicomputers, and presents a methodology for designing efficient algorithms within that class. The methodology was used to design a new polygon rendering algorithm that uses the frame-to-frame coherence of the screen image to evenly partition the rasterization at reasonable cost. An implementation of the algorithm on the Intel Touchstone Delta at Caltech, the largest multicomputer at the time, renders 3.1 million **triangles** per second. The rate was measured using a 806,640 **triangle** model and 512 i860 processors, and includes back-facing **triangles** . A similar algorithm is used in Pixel-Planes 5, a system that has specialized rasterization processors, and which, when introduced, had a benchmark score for the SPEC Graphics **Performance** Characterization Group "head" benchmark that was nearly four times faster than commercial workstations. The algorithm design methodology also identified significant **performance** improvements for Pixel-Planes 5.
    All fully parallel polygon rendering algorithms have a sorting step to redistribute primitives or fragments according to their screen location. The algorithm class mentioned above is one of four classes of parallel

rendering algorithms identified; the classes are differentiated by the type of data that is communicated between processors. The identified algorithm class, called sort-middle, sorts screen-space primitives between the transformation and rasterization.

The design methodology uses simulations and **performance** models to help make the design decisions. The resulting algorithm partitions the screen during rasterization into adaptively sized regions with an average of four regions per processor. The region boundaries are only changed when necessary: when one region is the rasterization **bottleneck** . On smaller systems, the algorithm balances the loads by assigning regions to processors once per frame, using the assignments made during one frame in the next. However, when 128 or more processors are used at high frame rates, the **load** balancing may take too long, and so static **load** balancing should be used. Additionally, a new all-to-all communication method improves the algorithm's **performance** on systems with more than 64 processors.

11/7/35   (Item 3 from file: 35)
DIALOG(R)File   35:DISSERTATION ABSTRACTS ONLINE
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01496449 ORDER NO: NOT AVAILABLE FROM UNIVERSITY MICROFILMS INT'L.
OPTOELECTRONIC PROCESSING AND NETWORKING: A DESIGN STUDY (SUPERCOMPUTING)
   Author: FRIETMAN, EUGENE EDUARD EDWIN
   Degree: DR.
   Year: **1995**
   Corporate Source/Institution: TECHNISCHE UNIVERSITEIT TE DELFT (THE
          NETHERLANDS) (0951)
   Source: VOLUME 57/03-C OF DISSERTATION ABSTRACTS INTERNATIONAL.
          PAGE 1003.   315 PAGES
   ISBN: 90-900-8690-0
   Location of Reference Copy: SECRETARIAT PHYSICS INFORMATICS, FACULTY OF
          APPLIED PHYSICS, LORENTZWEG 1, 2628 CJ DELFT, THE
          NETHERLANDS

     There is a broad consensus that major discoveries in key applications, the inventory of which has been made of in the report "Grand Challenges 1993: High **Performance** Computing and Communications" by the Committee on Physical, Mathematical and Engineering Sciences, would be within reach if computers 1000 times faster than today's conventional super computers exist, assuming equal progress in algorithms, software to exploit that computing power and **visualization** techniques to represent the results of the computations.
     Computers containing large numbers of processing **nodes** are required to study these "Grand Engineering Challenges". Such teraflop machines will be massively parallel, involving thousands of coupled **nodes** , solving problems containing trillions of data points. However large numbers of **nodes** linked by conventional busses suffer from communication congestions caused by bus contentions, which is known as the von Neumann **bottleneck** , as the bus must sequentialise many parallel data exchanges.
     Optical Processing, among which opto to electronic conversion, strives after as much as parallelism in storing and manipulating optical information. A new class of optically writable and electrically readable logic elements was introduced. Arrays of such elements, processed in bipolar as well as in CMOS, were realized with the IC group of the Faculty of Electrical Engineering.
     Optical Networking applied in such massively parallel computers not only implicates the choice of a suitable transport medium but rather aims at an optimum exploration and exploitation of its inherent parallelism. The investigation of optics inherent parallelism, involving billions of trajectories, is an important subject for study in the final years of the

twentieth century and beyond. It is foreseen that novel routing techniques can improve on **performance** of massively **parallel processors** when linking crates, **nodes** , chips or gates optically. The necessity of utilizing optical interconnects becomes crucial when large numbers of computing **nodes** are involved.

An optical free space data distributing system, enabling simultaneous communication between nine **nodes** , each of them producing 64 bits of information, was developed with the Institute of Applied Physics TPD/TNO.

The objective is to realize an Opto Electronic Processing & Networking system prototype, suitable to be implemented in a fully connected multiple instruction, multiple data stream (MIMD) architecture, containing 1024 or more computing **nodes** .

11/7/36 (Item 4 from file: 35)
DIALOG(R)File 35:DISSERTATION ABSTRACTS ONLINE
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01474311 ORDER NO: AADAA-I9610618
VISUAL ESTIMATION OF STRUCTURE IN RANKED DATA (POLYTOPES)
  Author: BAGGERLY, KEITH ALAN
  Degree: PH.D.
  Year: **1995**
  Corporate Source/Institution: RICE UNIVERSITY (0187)
  Chairman: DAVID W. SCOTT
  Source: VOLUME 56/12-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
          PAGE 6845. 116 PAGES

Ranked data arise when some group of judges is asked to rank order a set of n items according to some preference function. A judge's ranking is denoted by a vector x = $(x\sb1,...,x\sb{n}),$ where $x\sb{i}$ is the rank assigned to item i. If we treat these vectors as points in $\Re\sp{n}$, we are led to consider the geometric structure encompassing the collection of all such vectors: the convex hull of the n! points in $\Re\sp{n}$ whose coordinates are permutations of the first n integers. These structures are known as permutation polytopes.

The use of such structures for the analysis of ranked data was first proposed by Schulman $\lbrack65\rbrack$. Geometric constraints on the shapes of the permutation polytopes were later noted by McCullagh $\lbrack56\rbrack.$ Thompson $\lbrack77\rbrack$ advocated using the permutation polytopes as outlines for high-dimensional "histograms", and generalized the class of polytopes to deal with partial rankings (ties allowed).

Graphical representation of ranked data can be achieved by putting varying masses at the **vertices** of the generalized permutation polytopes. Each face of the permutation polytope has a specific interpretation; for example, item i being ranked first. The estimation of structure in ranked data can thus be transformed into geometric (visual) problems, such as the location of faces with the highest concentrations of mass.

This thesis addresses various problems in the context of such a geometric framework: the automation of graphical displays of the permutation polytopes; illustration and estimation of parametric models; and smoothing methods using duality--where every face is replaced with a point. A new way of viewing the permutation polytopes as projections of high-dimensional **hypercubes** is also given. The **hypercubes** are built as cartesian products of the $(\sbsp{2}{n})$ possible paired comparisons, and as such lead to methods for building rankings from collections of paired comparisons.

11/7/37 (Item 5 from file: 35)
DIALOG(R)File 35:DISSERTATION ABSTRACTS ONLINE

24 May 10, 2000 10:56

01219239   ORDER NO: AAD92-14510
IMPLEMENTATION OF RECURSIVE SHIFT-INVARIANT FLOW GRAPHS IN   PARALLEL
/PIPELINED   PROCESSING **ENVIRONMENTS (PIPELINED PROCESSING)**
   Author: HONG, CHUN PYO
   Degree: PH.D.
   Year: **1991**
   Corporate Source/Institution: GEORGIA INSTITUTE OF TECHNOLOGY (0078)
   Source: VOLUME 52/12-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
             PAGE 6564.   188 PAGES

     The objective of the research reported in this thesis is to develop a
set of techniques to automatically find rate optimal or near rate optimal
implementations in **parallel** /pipelined **processing**   environments for DSP
algorithms that are represented by recursive shift-invariant flow graphs.
The **parallel** /pipelined **processing**   environments are synchronous
parallel   processing systems that consist of one or more processors where
each processor could be internally pipelined. The shift-invariant flow
graph is a **graphical   representation** which describes the computational
structures of broad class of DSP algorithms at fine-grain level. Since the
node   execution   times in defining flow graphs are deterministic, this
research addresses compile time scheduling.
     The research in this thesis can be divided into three areas. First, an
instruction scheduling methodology for a single pipelined processor is
presented. In such case, the problem to be addressed is the scheduling of a
single instruction stream which controls all of the pipeline stages. The
goal of an automatic scheduler in this context is to rearrange the order of
instructions such that they are **executed** with minimum **time** and no
pipeline faults. In other words, sequences of instructions are ordered to
minimize the iteration period between successive iteration of defining flow
graphs.
     Second, a new class of multiprocessor system, called Clock-Skewed
Parallel   Processing system, is proposed. This system provides an elegant
solution to interprocessor communication problems multiprocessor system.
The interprocessor communication strategy described in this system is a
combination of a synchronous multiprocessor architecture, an associated
interprocessor communication architecture, and a multiprocessor compiler
which considers the interprocessor communication to be a scheduling
constraint. This system not only can handle the interprocessor
communications very efficiently but also can explicitly incorporate the
interprocessor communication time delay into the parallel scheduling model.
     Third, an instruction scheduling methodology for a multiple pipelined
processing system is presented. In this system, since more than one
pipelined processor is involved in **parallel   processing** , all the
processors must be interconnected in some manner. In such processing
environments, the interprocessor communications joins the instruction
scheduling as a major problem. This research presents a system scheduler
which combines the instruction scheduling methodology for a single
pipelined processor and the interprocessor communication strategy in the
clock-skewed **parallel   processing** system. This system has a simple
interprocessor communication structure which can provide good **performance**
and which results in scheduling constraints that can be reasonably
integrated into the searching algorithms of an optimal compiler.

   11/7/38   (Item 6 from file: 35)
DIALOG(R)File   35:DISSERTATION ABSTRACTS ONLINE

01164804   ORDER NO: AAD91-20229
TECHNIQUES FOR PARALLEL GEOMETRIC COMPUTATIONS (PARALLEL ALGORITHMS)

Author: KANKANHALLI, MOHAN S.
Degree: PH.D.
Year: **1990**
Corporate Source/Institution: RENSSELAER POLYTECHNIC INSTITUTE (0185)
Adviser: WM. RANDOLPH FRANKLIN
Source: VOLUME 52/02-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
          PAGE 932.   176 PAGES

     Parallel Computing is one solution for efficient processing of the large geometric databases encountered nowadays. This thesis presents the Uniform Grid and **Vertex** Neighborhood techniques for performing geometric operations in parallel. These techniques have several desirable properties. Their average **execution** **time** rises linearly with the sum of the input and output. They require little global information, which reduces the interprocessor communications cost. They exploit features of modern machines, such as a large flat address space, to avoid a log factor in times. The algorithms have simple data structures leading to ease of implementation. This research shows the broad applicability of these techniques by developing solutions for geometric problems in diverse application domains. These techniques have been used to develop efficient algorithms for Visible Surface Determination in **Visualization** and Iso-rectangle problems in VLSI. The Parallel Object-Space Visible Surface Determination algorithm has an expected time complexity of $O(\{n\over p\}$ + $k\{\rm log\}\sb2k)$ where n is the number of input edges and k the number of visible segments assuming a CREW PRAM model of computation with p processors. The implementation on a shared-memory Sequent Balance 21000 shows an average speedup of 10 using 15 **processors**. The **parallel** algorithm for computing the area of the union of a set of iso-rectangles has an expected time complexity of $O(\{n+k\over p\}$ + $log\$\sb2p\$)$ for a data set with n edges and k intersections on a p-processor machine. The Connection Machine implementation of the algorithm also exhibits good **performance**. This demonstrates the practical use of the techniques on different parallel architecture paradigms.

11/7/39   (Item 7 from file: 35)

01120389   ORDER NO: AAD90-24238
SCHEDULING, OPTIMIZATION AND CONTROL OF MULTIPURPOSE BATCH PLANTS
   Author: PATSIDOU, ELENI P.
   Degree: PH.D.
   Year: **1990**
   Corporate Source/Institution: UNIVERSITY OF NOTRE DAME (0165)
   Source: VOLUME 51/04-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
             PAGE 1954.   190 PAGES

     Multipurpose batch plants are often designed to concurrently produce a number of high-value products using a common collection of batch and semicontinuous processes. Because of their increased use in a number of emerging, small scale chemical industries, the design and planning of batch plants are receiving increased attention.
     The objective of this work is to develop a general model for the optimization and control of complex multipurpose batch plants.
     The system is modelled as a discrete event system by using Minimax Algebra which provides a framework to write linear equations that describe the **performance** of the plant. The state variables in these equations quantify the time at which designated events occur.
     A multipurpose batch plant is viewed as a network of activities. The sequencing graph of the system helps determining an effective set of variables that denote the **nodes** and the arcs of the **graph**. The

advantage of this **representation** is that the resulting model is very general and can describe many process features such as storage, equipment setup times, **parallel processing** at the same stage, and alternative production routes. The model of the system is formulated as a mixed-integer linear program. Binary variables denote the arcs of the graph and represent the processing sequence in each unit. Continuous variables denote the **nodes** of the graphs and represent the starting times of the activities.

The Model Predictive Control (MPC) of multipurpose batch plants is also discussed. MPC uses an explicit and separately identifiable model and optimizes an open-loop system to implement closed-loop control. The on-line calculation involves the solution of a mixed-integer linear program. The computed control consists of selecting the sequence, timing, and processing paths required to bring the system from a measured state to a final state.

11/7/40   (Item 8 from file: 35)
DIALOG(R)File   35:DISSERTATION ABSTRACTS ONLINE
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1036311   ORDER NO: AAD89-00774
QR FACTORIZATION ALGORITHMS FOR COARSE-GRAINED DISTRIBUTED SYSTEMS
  Author: BISCHOF, CHRISTIAN HEINRICH
  Degree: PH.D.
  Year: **1988**
  Corporate Source/Institution: CORNELL UNIVERSITY (0058)
  Source: VOLUME 49/10-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
            PAGE 4403.   105 PAGES

We present the techniques of adaptive blocking and incremental condition estimation which we believe to be useful for the computation of common matrix decompositions in high-**performance** environments. We apply these new techniques to algorithms for computing the Householder QR factorization with and without pivoting on a coarse-grained distributed system. For reasons of portability, we use a pipelined scheme on a ring of processors as the basis of our algorithms.

To take advantage of possible floating point hardware on each **node** we develop a blocked version of the pipelined Householder QR algorithm that employs the compact WY **representation** for products of Householder **matrices** . While a strategy involving blocks of fixed width leads to increased floating point utilization per **node** , it also leads to increased **load** imbalance. To reconcile this tradeoff we introduce a variable width blocking strategy based on a model of the critical path of the algorithm. The resulting adaptive blocking strategy provides for good floating point **performance** per **node** while maintaining overall **load** balance. Experimental results on the Intel iPSC **hypercube** show that the adaptive blocking strategy performs indeed better than any fixed width blocking strategy.

In the second part of our thesis we develop methods for introducing pivoting into the distributed QR factorization algorithm. Incorporating the traditional column pivoting strategy in a straightforward manner introduces a global synchronization constraint which results in increased communication overhead. A strictly local pivoting scheme avoids the resulting loss in efficiency, but has to be monitored for reliability. To this end, we introduce an incremental condition estimator which allows us to update the estimate of the smallest singular value of an upper **triangular** matrix R as new columns are added to R. The update requires only $O(n)$ flops and the storage of $O(n)$ words between successive steps. Experiments indicate that the incremental condition estimator is reliable despite its small computational cost. Using the incremental condition estimator we are then able to guard against the selection of troublesome pivot columns in our local pivoting scheme at little extra cost. Simulation results show that the resulting algorithm is about as reliable as the

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traditional QR factorization algorithm with column pivoting.

11/7/41   (Item 9 from file: 35)
DIALOG(R)File 35:DISSERTATION ABSTRACTS ONLINE
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0991554 ORDER NO: AAD88-08194
ON MAPPING ALGORITHMS ONTO PROCESSOR ARRAYS
   Author: SHEN, WEICHENG
   Degree: PH.D.
   Year: **1987**
   Corporate Source/Institution: RENSSELAER POLYTECHNIC INSTITUTE (0185)
   Source: VOLUME 49/04-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
            PAGE 1325. 128 PAGES

     Two design procedures for parallel computers have been developed,
which map computations onto processor arrays. The first is a procedure that
programs a **processor   array** for computing a given expression. It
consists of the following steps: (1) determining the type of expressions
that can be evaluated by a given **processor   array** ; (2) setting the
processors in the **processor   array** to carry out a computation within its
computation space. This mapping procedure has been demonstrated for
mesh-connected processing networks.
     The second procedure is a contraction mapping procedure that derives a
target **processor   array** from a directed acyclic **graph   representation**
of a program. This procedure consists of the following steps: (1)
representing the given problem by a homogenous program graph; (2)
partitioning the **vertices** of the graph into subsets such that all the
vertices in the same subset will be executed by one processor; (3)
characterizing the algebraic relations of delays between computations by a
fundamental loop matrix; (4) establishing a linear function of delays as a
performance metric and solving the delays that minimize the linear cost
function by linear programming; (5) constructing a contracted graph from
that program graph. The contracted graph delineates the target **processor
array** that computes the given problem. This contraction mapping procedure
is applied to a variety of problems, including algebraic computations and
character string processing.

11/7/42   (Item 10 from file: 35)
DIALOG(R)File 35:DISSERTATION ABSTRACTS ONLINE
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952870 ORDER NO: AAD87-10247
**A DATA-DRIVEN DATABASE MODEL AND ITS IMPLEMENTATION ON A HIGHLY-PARALLEL
ARCHITECTURE**
   Author: HARTMANN, ROBERT LAVERNE
   Degree: PH.D.
   Year: **1987**
   Corporate Source/Institution: UNIVERSITY OF CALIFORNIA, IRVINE (0030)
   Source: VOLUME 48/01-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
            PAGE 186. 144 PAGES

     The search for computer architectures utilizing large numbers of
processing elements and their application to suitable problems has been a
continual quest for many researchers. This dissertation presents results of
an analysis of a multiprocessor architecture applied to the problem of
database management.
     The database problem is first re-stated in terms of a new data
model, the Active **Graph** Model, which employs a **graphical
representation** for data (**nodes**) and relationships (arcs) in addition to

concepts from the dataflow model of computation to exploit the **parallel processing** power of the architecture. The **nodes** of the graph are 'active' elements which respond to requests in the form of tokens traveling along the arcs. This data model and its query language are shown to be relationally complete and therefore equivalent in expressive power to the Relational Model.

A mesh-connected **array** of **processing** elements forms the basis for the architecture. The **nodes** and arcs of the model are mapped onto the architecture and practical algorithms are defined for distributing requests, data manipulation, and for sorting and reporting of results. The functionality of these algorithms is verified and the **performance** characteristics of the system are measured through an implementation of the algorithms on simulated hardware using a standardized evaluation methodology.

The results of the experiments demonstrate that large numbers of processors can be used effectively given a sufficiently large problem. Additionally, under-utilized processing capability can be used by multiple simultaneous requests. Finally, the system is not plagued by interprocessor communications **bottlenecks** which have been identified in other such systems.

11/7/43   (Item 11 from file: 35)
DIALOG(R)File 35:DISSERTATION ABSTRACTS ONLINE
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942226 ORDER NO: AAD87-02049
A FRAME-BASED 3D VISION SYSTEM (PARALLEL   PROCESSING,   3- D **SURFACE** REPRESENTATION, **STRUCTURED LIGHT)**
   Author: HSIAO, MENG-LING
   Degree: PH.D.
   Year: **1986**
   Corporate Source/Institution: UNIVERSITY OF PITTSBURGH (0178)
   Source: VOLUME 47/10-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
            PAGE 4255. 162 PAGES

A Frame-Based Image Processing (FBIP) system is designed to provide a high **throughput** computation rate for the applications in image processing and pattern recognition. The detailed configuration of the processing element and the organization of the memory cell are described. A mathematical model is proposed to describe both the hardware architecture and the parallelism of the software. Both the logical and arithmetical Frame-Based operations are accomplished on a pixel-by-pixel basis. According to the geometric properties of the memory cell connection, the parallelism of the local processing can be achieved through the successively shift and accumulate technique. Experimental results of the Frame-Based local convolution, the Frame-Based edge operation and the Frame-Based cellular operation are presented.

A multi-stage vision system is described to understand the three-dimensional surface characteristics from multiple two-dimensional images. The structured lighting control technique associated with the orthographics projection model is applied such that the computation of the surface gradient can be accomplished with Frame-Based operations. Analyses are conducted for the estimation of surface orientation with various lighting arrangements. Recommendations for simple and general approaches are also provided. Furthermore, an element type structure is utilized by using the gradient image to describe the surface profile. The **triangular** element, based on the equigradient contour, is chosen as the basic unit for surface representation.

11/7/44   (Item 1 from file: 103)
DIALOG(R)File 103:Energy SciTec
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03516679   EDB-93-095554
Title: Program partitioning for NUMA multiprocessor computer systems
Author(s): Wolski, R.; Feo, J. (Lawrence Livermore National Lab., CA
    , (United States))
Title: Proceedings of the second SISAL users' conference
Author(s)/Editor(s): Feo, J.T.; Frerking, C.; Miller, P.J. (eds.)
Corporate Source: Lawrence Livermore National Lab., CA (United States)
Conference Title: 2. sisal users' conference
Conference Location: San Diego, CA (United States)   Conference Date: 4-5
    Oct 1992
Publication Date: Dec **1992**   p 111-137   (273 p)
Report Number(s): CONF-9210270--
Order Number: DE93008019
Contract Number (DOE): W-7405-ENG-48
Language: English
Availability: OSTI; NTIS
Abstract: An important part of parallel programming is program partitioning
    and scheduling. Partitioning is the separation of program operations
    into sequential tasks, and scheduling is the assignment of tasks to the
    processors of a computer system. To be effective, automatic methods
    require an accurate representation of the model of computation and the
    target architecture. Current partitioning methods assume the
    macro-dataflow model of computation and the homogeneous/two-level
    architectural model. The former is typically represented as a directed,
    acyclic graph of computation **nodes** and communication edges. The edges
    map directly to communication channels, but not read/write memories.
    Consequently, current methods optimize assuming the presence of
    communication channels, and not the complex memory systems of NUMA
    architectures-they fail to optimize for a critical component of these
    architectures. In this paper, we extend the conventional **graph
  representation** of the macro-dataflow model to enable mapping
    heuristics to work with a NUMA architectural model. We describe two
    such heuristics. Simulated **execution**   **times** of programs show that
    our model and heuristics generate higher quality program mappings than
    current methods.

11/7/45   (Item 2 from file: 103)
DIALOG(R)File 103:Energy SciTec
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03330550   NOV-92-007320; EDB-92-084848
Title: The data transport computer A 3-dimensional massively parallel SIMD
    computer
Author(s): Jackson, J.H. (WAVETRACER, Inc., Cary, NC (US))
Title: Proceedings of the 36th IEEE computer international conference
Conference Title: COMPCON '91: 36th Institute of Electrical and Electronic
    Engineers (IEEE) Computer Society international conference
Conference Location: San Francisco, CA (United States)   Conference Date:
    25 Feb - 1 Mar 1991
Publisher: Piscataway, NJ (United States) IEEE Service Center
Publication Date: **1991**   p 264-269   (601 p)
Report Number(s):   CONF-910263--
Language: In English
Availability: IEEE Service Center, 445 Hoes Ln., Piscataway, NJ 08854
    (United States)
Abstract: Mathematical models for predicting the behavior of physical

phenomena by computer, as well as for other complex applications, are often restricted to two spatial dimensions to limit the computing **resources** required to analyze them. However, real world phenomena occur in a three-dimensional space. This paper describes a computer that has been built primarily to support both three-dimensional simulation of physical phenomena, as well as other applications that require **three -dimensional** models, and **visualization** of the results as volume data. This computer is a massively parallel SIMD machine whose processors are interconnected in a three-dimensional rectangular lattice, together with a controller that extends this lattice to a virtual lattice with many more **nodes** than there are processors. It is called the Data Transport Computer because its interprocessor communication structure is capable of moving large amounts of data in parallel not only among its processors, but also to and from 110 devices.

11/7/46   (Item 3 from file: 103)
DIALOG(R)File 103:Energy SciTec
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02975139   NOV-90-044057; EDB-91-008764
Title: Costs of quadtree representation **of nondense** matrices
Author(s): Wise, D.S.; Franco, J. (Indiana Univ., Bloomington, IN (USA).
    Dept. of Computer Science)
Source: Journal of Parallel and Distributed Computing (USA) v 9:3.
Coden: JPDCE ISSN: 0743-7315
Publication Date: Jul **1990**   p 282-296
Contract Number (Non-DOE): DCR84-05241
Language: In English
Abstract: The quadtree **representation** of **matrices** is a uniform
    representation for both sparse and dense **matrices** which can
    facilitate shared manipulation on multiprocessors. This paper presents
    worst-case and average-case **resource** requirements for storing and
    retrieving familiar families of patterned matrices: packed, symmetric,
    triangular , Toeplitz, and banded. Using this representation it
    compares **resource** requirements of three kinds of permutation
    matrices, as examples of nondense, unpatterned matrices. Exact values
    for the shuffle and bit-reversal permutations (as in the fast Fourier
    transform) and tight bounds on the expected values from purely random
    permutations are derived. Two different measures, {ital density} and
    {ital sparsity}, are proposed from these values. Analysis of quadtree
    matrix addition relates density of addends to space bounds on their sum
    and relates their sparsity to time bounds for computing that sum.

11/7/47   (Item 4 from file: 103)
DIALOG(R)File 103:Energy SciTec
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02759809   EDB-89-150849
Title: Multiple crossbar network: A switched high-speed local network
Author(s)/Editor(s): Hoebelheinrich, R.; Thomsen, R.
Corporate Source: Los Alamos National Lab., NM (USA)
Sponsoring Organization: DOE/MA
Conference Title: 14. conference on local computer networks
Conference Location: Minneapolis, MN (USA)   Conference Date: 10-12 Oct
    1989
Publication Date: **1989**   (16 p)
Report Number(s): LA-UR-89-3155   CONF-8910209--2
Order Number: DE90001839
Contract Number (DOE): W-7405-ENG-36

31 May 10, 2000 10:56

Language: In English
Availability: NTIS, PC A03/MF A01 - OSTI; GPO Dep.
Abstract: The Multiple Crossbar Network (MCN) is a prototype High-Speed
    Local Network at the Los Alamos National Laboratory. It will
    interconnect supercomputers, network servers and workstations from
    various commercial vendors. The MCN can also serve as a backbone for
    message **traffic** between local area networks. The MCN is a switched
    local network of switching **nodes** called **Cross -Point** Stars (CPs).
    Hosts and CPs are connected by 800-Mbit/s (100-Mbyte/s) point-to-point
    ANSI High-Speed Channels. CPs include RISC-based network protocol
    processors called Crossbar Interfaces and a switching core called the
    Crossbar Switch. Protocols include physical, data link, intranet, and
    network access functionality. Various internet and transport protocols
    are intended to run above the MCN protocol suite. A network management
    and simple naming service is also included within the Los Alamos
    Network Architecture. Immediate applications include **visualization** .
    The MCN is intended to also serve as a framework for multicomputer
    applications. 36 refs., 10 figs.

  11/7/48   (Item 5 from file: 103)
DIALOG(R)File 103:Energy SciTec

02366538   EDB-89-112510
Author(s): Benner, R.E.
Title: Parallel graphics algorithms on a 1024-processor hypercube
Corporate Source: Sandia National Labs., Albuquerque, NM (USA)
Conference Title: 4. hypercube, concurrent computers and applications
Conference Location: Monterey, CA, USA   Conference Date: 6-8 Mar 1989
Publication Date: **1989**   p 13
Report Number(s): SAND-89-0550C; CONF-890372-12
Order Number: DE89015492
Contract Number (DOE): AC04-76DP00789
Note: Portions of this document are illegible in microfiche products
Language: English
Availability: NTIS, PC A03/MF A01 - OSTI; 1.
Abstract: We have developed four parallel **graphics** algorithms for
    visualization of complex problems in PDE simulations, radar
    simulation, and other large applications on a 1024-**node** ensemble with
    a 16-**node** graphics device. We discuss the impact of system parameters
    on algorithm development and **performance** . Algorithmic issues include
    multistage routing of graphics data through the ensemble, non-
    hypercube mappings from the ensemble to the graphics system,
    synchronization between ensemble and graphics **nodes** , and
    synchronization between graphic **nodes** . These issues apply to both the
    present and anticipated future systems which combine highly parallel
    ensembles and parallel I/O devices. ''Best'' solutions are described
    for routing, mapping and synchronization on the current hardware.
    Implications are discussed for future hardware and software for
    massively parallel computers. 6 refs., 2 figs., 2 tabs.

  11/7/49   (Item 6 from file: 103)
DIALOG(R)File 103:Energy SciTec

02329766   GRA-89-80383; EDB-89-075508
Author(s): Deprit, E.M.
Title: Implementing Recurrent Back Propagation on the Connection Machine.
    Final report
Corporate Source: Naval Research Lab., Washington, DC (USA)

Publication Date: 2 Dec **1988**   p 111
Report Number(s): AD-A-203796/8/XAB; NRL-9167
Language: English
Availability: NTIS, PC A06/MF A01.
Abstract: Pineda's Recurrent Back-Propagation algorithm for neural networks
    was implemented on the Connection Machine, a massively **parallel**
    processor . Two fundamentally different graph architectures underlying
    the nets were tested - one based on arcs, the other on **nodes** .
    Confirming the predominance of communication over computation,
    performance measurements underscore the necessity to make connections
    the basic unit of **representation** . Comparisons between these **graphs**
    algorithms lead to important conclusions concerning the parallel
    implementation of neural nets in both software and hardware.

 11/7/50   **(Item 7 from file: 103)**
DIALOG(R)File 103:Energy SciTec

02314651   NOV-89-048312; EDB-89-060391
Title: Parallel   processing **for image computing**
Author(s): Piol, A.; Johnson, H.L.
Affiliation: AT and T Pixel Machines, Crawfords Corner Road, 4K-202,
    Holmdel, NJ (US)
Title: Proceedings of the fourth SCS multiconference on multiprocessors and
    array   processors
Conference Title: Multiprocessors and array processors
Conference Location: San Diego, CA, USA   Conference Date: 3 Feb 1988
Publisher: Society for Computer Simulation,San Diego, CA
Publication Date: **1988**   p 91-93 v
Report Number(s): CONF-880295-
Language: English
Abstract: Image computing is a computationally intensive task, and in order
    to meet the increasing **performance** needs of sophisticated users, new
    hardware architectures must be developed along with advancing software
    algorithms. AT and T Pixel Machines has used a new, highly parallel
    architecture that incorporates both a pipeline of 9 to 18 processing
    nodes and a parallel array of 16 to 64 processing **nodes** in its new
    image computers, the PXM 900 Series. The PXM 900 provides up to 820
    MFLOPS of peak processing power for applications such as the rendering
    and animation of **3D** **graphics** , data **visualization** , **image**
    processing, and a variety of scientific applications. Each processing
    node is based on a high speed, floating point, programmable processor.
    This programmability ensures that the hardware can adapt to new
    advances in software algorithms. The architecture is modular so that
    users can update to higher models as their **performance** and image
    memory needs increase.

 11/7/51   **(Item 8 from file: 103)**
DIALOG(R)File 103:Energy SciTec

02033195   NOV-87-074521; EDB-87-161150
Title: Mapping data flow programs on a VLSI array **of** processors
Author(s): Mendelson, B.; Silberman, G.M.
Affiliation: Technion - Israel Institute of Technology, Haifa
Title: Proceedings of the 14th annual international symposium on computer
    architecture
Conference Title: 14. annual international symposium on computer
    architecture
Conference Location: Pittsburgh, PA, USA   Conference Date: 2 Jun 1987

Publisher: IEEE Service Center,Piscataway, NJ
Publication Date: **1987**   p 72-80
Report Number(s): CONF-8706138-
Language: English

Abstract: With the advent of VLSI, relatively large processing arrays may
    be realized in a single VLSI chip. Such regularly structured arrays
    take considerably less time to design and test, and fault-tolerance can
    easily be introduced into them. However, only a few computational
    algorithms which can effectively use such regular arrays have been
    developed so far. The authors present an approach to mapping arbitrary
    algorithms, expressed as programs in a data flow language, onto a
    regular array of data-driven processors implemented by a number of VLSI
    chips. Each chip contains a number of processors, interconnected by a
    set of regular paths, and connected to processors in other similar
    chips to form a large array. This array is thus tailored to perform a
    specific computational task, as an attached processor in a larger
    system. The data flow program is first translated into a **graph
    representation** , the data flow **graph** , which is then mapped onto a
    finite but (theoretically) unbounded **array** of identical **processors** .
    Each **node** in the graph represents an operation which can be performed
    by an individual **processor** in the **array** . Therefore, the mapping
    operation consists of assigning **nodes** in the graph to **processors**   in
    the **array** , and defining the connections between the processors
    according to the arcs in the graph. The last step consists of
    partitioning the unbounded array into a number of segments, to account
    for the number of processors which fit in a single VLSI chip.

 11/7/52   (Item 9 from file: 103)
DIALOG(R)File 103:Energy SciTec

01963988   NOV-87-056516; EDB-87-091655
**Title: Using cellular automata in graph theory modelling: A high
    performance solution of the Hamilton problem**
Author(s): Perez, J.C.;   Castanet, R.; Luker, P.A.;   Adelsberger, H.H.
Affiliation: IBM France, Bordeaux, Robotics Center, Route de Canejan 33610
    Cestas
Title: Intelligent simulation environments
Series/Collection Title: Simulation Series. Volume 17 Number 1
Conference Title: Society for Computer Simulation (SCS) multiconference
Conference Location: San Diego, CA, USA   Conference Date: 23 Jan 1986
Publisher: Society for Computer Simulation,San Diego, CA
Publication Date: **1986**   p 3-8
Report Number(s): CONF-860119-
Language: English

Abstract: After general considerations on a parallel approach of graph
    theory problems, the authors present a specific problem: ''To find
    hamiltonian circuits in a 3-**vertex** connected cubic graph''. This
    problem is similar to the ''Travelling Salesman Problem''. They
    present a parallel Knowledge **Representation** of the **graph** . The
    parallel algorithm uses parallel Propagation of Cellular Automata. This
    Exhaustive approach is combined with a powerful Heuristic method. The
    result is a powerful polynomial algorithm which finds Hamiltonian
    circuits in complex graphs. Meanwhile, an open-problem is discussed
    and research of cases where this algorithm fails is reported.

 11/7/53   (Item 1 from file: 2)
DIALOG(R)File   2:INSPEC

5608636   INSPEC Abstract Number: C9707-5220P-023
  Title: A modular massively parallel   processor **for volumetric**
  visualisation **processing**
  Author(s): Krikelis, A.
  Author Affiliation: Aspex Microsyst. Ltd., Brunel Univ., Uxbridge, UK
  Conference Title: High Performance Computing for Computer Graphics and
Visualisation. Proceedings of the International Workshop   p.101-24
  Editor(s): Chen, M.; Townsend, P.; Vince, J.A.
  Publisher: Springer-Verlag, Berlin, Germany
  Publication Date: 1996 Country of Publication: Germany   xvi+287 pp.
  ISBN: 3 540 76016 4   Material Identity Number: XX95-01869
  Conference Title: Proceedings of International Workshop on High
Performance Computing for Computer Graphics and Visualization
  Conference Sponsor: High Educ. Funding Council for Wales
  Conference Date: 3-4 July 1995   Conference Location: Swansea, UK
  Language: English   Document Type: Conference Paper (PA)
  Treatment: Practical (P)

  Abstract: A Modular Massively **Parallel Processor** capable of achieving
real-time/interactive   **performance**   for   volumetric **visualisation**
applications is presented in this paper. The processor comprises identical
SIMD processing **nodes** , which can be configured through a Data Transfer
Network to support SIMSIMD and MIMSIMD configurations, while supporting
independent   Data I/O of 80 Mbytes/sec per **node** . For volumetric
visualisation   computation the system operates in SIMSIMD configuration
with voxel slices equally distributed to each **node** . Data formation and
classification which are based on traditional image processing techniques
are performed with data local to each **node** using the SIMD computational
power of it, which is implemented using the Associative String Processor
(ASP). For data manipulation computation, each **node** accesses data from
remote **nodes** (with all the **nodes** using similar access patterns) through
the Data Transfer Network. Once access to remote **nodes** has been achieved
the data are processed on the ASP on one (or a group of) slice(s) at a time
for data viewing (i.e. shading and front-to-back composition). (27 Refs)

  11/7/54   (Item 2 from file: 2)

5576776   INSPEC Abstract Number: C9706-4240P-034
  **Title: Architecture-independent locality-improving transformations of
computational graphs embedded in k-dimensions**
  Author(s): Chao-Wei Ou; Gunwani, M.; Ranka, S.
  Author Affiliation: Sch. of Comput. & Inf. Sci., Syracuse Univ., NY, USA
  Conference Title: Conference Proceedings of the 1995 International
Conference on Supercomputing   p.289-98
  Publisher: ACM, New York, NY, USA
  Publication Date: 1995 Country of Publication: USA   xii+448 pp.
  ISBN: 0 89791 728 6   Material Identity Number: XX95-01418
  U.S. Copyright Clearance Center Code: 0 89791 728 6/95/000.$3.50
  Conference Title: Proceedings of 9th ACM International Conference on
Supercomputing
  Conference Sponsor: ACM
  Conference Date: 3-7 July 1995   Conference Location: Barcelona, Spain
  Language: English   Document Type: Conference Paper (PA)
  Treatment: Theoretical (T)
  Abstract: A large number of data-parallel applications can be represented
as computational graphs from the perspective of parallel computing. The
 nodes of these graphs represent tasks that can be executed concurrently,
while the edges represent the interactions between them. Further, the
computational graphs derived from many applications are such that the

vertices correspond to multi-dimensional coordinates, and the interaction between computations is limited to **vertices** that are physically proximate. The authors show that graphs with these properties can be transformed into simple architecture-independent representations that encapsulate the locality in these **graphs** . This **representation** allows a fast mapping of the computational graph onto the underlying architecture at the **time** of **execution** . This is necessary for environments where available computational **resources** can be determined only at the **time** of **execution** or that change during execution. (32 Refs)
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11/7/55   (Item 3 from file: 2)
DIALOG(R)File   2:INSPEC
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5484482   INSPEC Abstract Number: B9703-6140C-156, C9703-1250-069
  Title: **Morphological operations on images represented by quadtrees**
  Author(s): Reitseng Lin; Wong, E.K.
  Author Affiliation: Dept. of Comput. & Inf. Sci., Polytech. Univ., Brooklyn, NY, USA
  Conference Title: 1996 IEEE International Conference on Acoustics, Speech, and Signal Processing Conference Proceedings (Cat. No.96CH35903)
Part vol. 4   p.2203-6 vol. 4
  Publisher: IEEE, New York, NY, USA
  Publication Date: 1996 Country of Publication: USA   6 vol. lvii+3588 pp.
  ISBN: 0 7803 3192 3   Material Identity Number: XX96-02719
  U.S. Copyright Clearance Center Code: 0 7803 3192 3/96/$5.00
  Conference Title: 1996 IEEE International Conference on Acoustics, Speech, and Signal Processing Conference Proceedings
  Conference Sponsor: Signal Process. Soc. IEEE
  Conference Date: 7-10 May 1996   Conference Location: Atlanta, GA, USA
  Language: English   Document Type: Conference Paper (PA)
  Treatment: Theoretical (T)
  Abstract: This paper presents an algorithm to directly perform morphological operations on images represented by quadtrees and produce the dilated/eroded images, also represented by quadtrees. As in many other algorithms that execute on the quadtree **representation** of an **image** , the **execution** **time** is proportional to the number of **nodes** in the quadtree, rather than to the number of pixels in the original image array. In our algorithm, only black **nodes** have to be processed for dilation, and only white **nodes** have to be processed for erosion. We also performed experiments to show that the **execution** **time** for binary images that can be effectively represented by quadtrees can be significantly reduced, compared to direct computation on the original image arrays. (8 Refs)
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11/7/56   (Item 4 from file: 2)
DIALOG(R)File   2:INSPEC
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5050641   INSPEC Abstract Number: B9510-6210M-041, C9510-6150G-033
  Title: **DIVIDE: Distributed visual display of the execution of asynchronous, distributed algorithms on loosely-coupled** parallel processors
  Author(s): Morrow, T.M.; Ghosh, S.
  Author Affiliation: Oracle Corp., Redwood Shores, CA, USA
  Conference Title: Proceedings Visualization '93. (Cat. No.93CH3354-8)
p.166-73
  Editor(s): Nielson, G.M.; Bergeron, D.

Abstract: The issue of monitoring the execution of asynchronous,
distributed algorithms on loosely-coupled **parallel processor** systems,
is important for the purposes of (i) detecting inconsistencies and flaws in
the algorithm, (ii) obtaining important **performance** parameters for the .
algorithm, and (iii) developing a conceptual understanding of the
algorithm's behavior, for given input stimulus, through **visualization** .
For a particular class of asynchronous distributed algorithms that may be
characterized   by   independent   and concurrent entities that execute
asynchronously on multiple processors and interact with one another through
explicit messages,   the following reasoning applies. Information about the
flow of messages and the activity of the processors may contribute
significantly towards the conceptual understanding of the algorithm's
behavior and the functional correctness of the implementation. The
computation and subsequent display of important parameters, based upon the
execution of the algorithm, is an important objective of DIVIDE. For
instance,   the mean and standard deviation values for the propagation delay
of ATM cells between any two given Broadband-ISDN (BISDN) **nodes** in a
simulation of BISDN network under stochastic input stimulus, as a function
of time, are important clues to the degree of congestion in the
Broadband-ISDN network. Although the execution of the algorithm typically
generates   high   resolution   data,   often,   a   coarse-level **visual
representation**   of the data may be useful in facilitating the conceptual
understanding of the behavior of the algorithm. DIVIDE permits a user to
specify a resolution less than that of the data from the execution of the
algorithm, which is then utilized to coalesce the data appropriately. Given
that this process requires significant computational power, for efficiency,
DIVIDE distributes the overall task of visual display into a number of user
specified workstations that are configured as a loosely-coupled **parallel
processor** . DIVIDE has been implemented on a heterogeneous network of SUN
sparc 1 + , sparc 2, and 3/60 workstations and **performance** measurements
indicate significant improvement over that of a uniprocessor-based visual
display. (24 Refs)

11/7/57   (Item 5 from file: 2)
DIALOG(R)File   2:INSPEC
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4946681   INSPEC Abstract Number: C9506-5630-007
 Title: **GigaView** parallel **image** server performance **analysis**
   Author(s): Gennart, B.A.; Krummenacher, B.; Landron, L.; Hersch, R.D.
   Author Affiliation: Ecole Polytech. Federale de Lausanne, Switzerland
   Conference Title: Transputer Applications and Systems'94. Proceedings of
the 1994 World Transputer Congress   p.120-35
   Editor(s): de Gloria, A.; Jane, M.R.; Marini, D.
   Publisher: IOS Press, Amsterdam, Netherlands
   Publication Date: 1994 Country of Publication: Netherlands   xi+1009
pp.
   Conference Title: Transputer Applications and Systems'94. Proceedings of
the 1994 World Transputer Congress

Conference Sponsor: Transputer Consortium; SGS-Thomson Microelectron.; Eur. Union; Italian Transputer User Group
    Conference Date: 5-7 Sept. 1994   Conference Location: Como, Italy
    Language: English   Document Type: Conference Paper (PA)
    Treatment: Applications (A); Practical (P)
    Abstract: Professionals in various fields such as medical imaging, biology and civil engineering require rapid access to huge amounts of uncompressed pixmap image data. Multi-media interfaces further increase the need for large image databases. In order to fulfill these requirements, the GigaView **parallel** image **server** architecture relies on arrays of intelligent disk **nodes** , each disk **node** being composed of one processor and one disk. This contribution analyzes through simulation and experimentation the behavior of the GigaView under single and multiple requests, and compares it to the behavior of RAID servers. It evaluates **image visualization** window access times under various parameters such as **load** factors and the number of cooperating disk **nodes** . Under single request, the GigaView image server can be modeled as a single high-**throughput** low-latency secondary storage device. Under multiple requests, the notions of utilization and maximum sustainable **throughput** define accurately the behavior of the GigaView. (9 Refs)

    11/7/58   (Item 6 from file: 2)

4930028   INSPEC Abstract Number: C9506-4185-001
    Title: Recursive spectral algorithms for automatic domain partitioning in parallel finite element analysis
    Author(s): Shang-Hsien Hsieh; Paulino, G.H.; Abel, J.F.
    Author Affiliation: Sch. of Civil Eng., Purdue Univ., West Lafayette, IN, USA
    Journal: Computer Methods in Applied Mechanics and Engineering vol.121, no.1-4   p.137-62
    Publication Date: March 1995 Country of Publication: Netherlands
    CODEN: CMMECC ISSN: 0045-7825
    U.S. Copyright Clearance Center Code: 0045-7825/95/$09.50
    Language: English   Document Type: Journal Paper (JP)
    Treatment: Theoretical (T)
    Abstract: Several domain partitioning algorithms have been proposed to effect **load** -balancing among **processors** in **parallel** finite element analysis. The recursive spectral bisection (RSB) algorithm has been shown to be effective. However, the bisection nature of the RSB results in partitions of an integer power of two, which is too restrictive for computing environments consisting of an arbitrary number of processors. The paper presents two recursive spectral partitioning algorithms, both of which generalize the RSB algorithm for an arbitrary number of partitions. These algorithms are based on a graph partitioning approach which includes spectral techniques and **graph representation** of finite element meshes. The 'algebraic connectivity vector' is introduced as a parameter to assess the quality of the partitioning results. Both **node** -based and element-based partitioning strategies are discussed. The spectral algorithms are also evaluated and compared for coarse-grained partitioning using different types of structures modelled by 1D, 2D and 3D finite elements. (28 Refs)

    11/7/59   (Item 7 from file: 2)

04164897   INSPEC Abstract Number: C9207-7430-003
  **Title: A discrete event simulator of communication algorithms in
interconnection networks**
  Author(s): Grammatikakis, M.D.; Jung-Sing Jwo
  Author Affiliation: Lab. de l'Inf. du Parallelisme, Ecole Normale
Superieure de Lyon, France
  Conference Title: STACS 92. 9th Annual Symposium on Theoretical Aspects
of Computer Science. Proceedings   p.609-10
  Editor(s): Finkel, A.; Jantzen, M.
  Publisher: Springer-Verlag, Berlin, Germany
  Publication Date: 1992 Country of Publication: West Germany   xiv+620
pp.
  ISBN: 3 540 55210 3
  Conference Date: 13-15 Feb. 1992   Conference Location: Cachan, France
  Language: English   Document Type: Conference Paper (PA)
  Treatment: Practical (P)

  Abstract: The   authors   demonstrate   a   discrete-event   simulator   for
evaluating the **performance** of various routing algorithms (probabilistic
and   deterministic)   in   both   multicomputers,   and   multistage   parallel
interconnection   networks.   This   simulator   can   route   packets   in   a   mesh,   a
generalized **hypercube** , or a star graph. It can also realize connection
requirements   for   a   given   permutation, on an omega network, an augmented
data   manipulator,   or   a   multistage   circuit-switched   **hypercube** .   Current
multicomputer, and multiprocessor designs tend to become increasingly
complex. Therefore, it is very difficult to analytically evaluate their
 performance   , and simulator tools become very useful. The authors are
motivated to design a flexible and efficient simulator of various routing
schemes, on both multicomputer, and multiprocessor architectures. Such
parallel systems usually incorporate a highly symmetric interconnection
network.   By   exploiting   this   symmetry,   they   avoid   an   explicit
 representation   (adjacency list, or **matrix**) of the underlying network.
Instead,   the   communication   algorithm   is   'smart' to route messages along
adjacent **nodes** . The implementation is also event-driven, which is faster
and easier to parallelize. The available options are described and a
glimpse provided of current results and future extensions of this tool. (
15 Refs)

  11/7/60   (Item 8 from file: 2)
DIALOG(R)File   2:INSPEC
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04137371   INSPEC Abstract Number: C9206-5220P-009
  Title: PARAM architecture, programming environment and applications
  Author(s): Bhatkar, V.P.
  Author Affiliation: Centre for Dev. of Adv. Comput., Poona Univ., Pune,
India
  Conference Title: Applications of Transputers 3. Proceedings of the Third
International Conference on Applications of Transputers   p.48-59
  Editor(s): Durrani, T.S.; Sandham, W.A.; Soraghan, J.J.; Forbes, S.M.
  Publisher: IOS, Amsterdam, Netherlands
  Publication Date: 1991 Country of Publication: Netherlands   821 pp.
  Conference Sponsor: UK SERC/DTI Initiative on the Eng. Appl. Transputers;
IEEE; IEE; IOP; et al
  Conference Date: 28-30 Aug. 1991   Conference Location: Glasgow, UK
  Language: English   Document Type: Conference Paper (PA)
  Treatment: Practical (P)
  Abstract: PARAM is a multi-user, reconfigurable, scalable, MIMD parallel
computer with peak **performance** exceeding 1 GFLOPS, developed under the
Indian parallel computing initiative. Some notable features of PARAM are
coherent integration of high-**performance** **vector** and signal **processing**

nodes , orthogonal supervisory and control bus, innovative packaging of compute cluster, and high-bandwidth high-**capacity** parallel disk array support. PARAM is endowed with an advanced integrated parallel programming environment, PARAS. PARAS is aimed at a host/back-end hardware model and provides an environment that efficiently harnesses the power of **parallel processing** offered by distributed memory, message passing machines such as PARAM. The host resident part of PARAS provides an easy-to-use environment for developing parallel programs as well as interactive user interfaces for profiling and debugging. Functions on the back-end, include, file and process management, message communication between remote tasks, mutual exclusion of shared variables and support for process farming, scientific data **visualisation** , debugging and profiling. PARAS offers a high bandwidth parallel file system which uses block declustering of files across multiple I/O **nodes** and spindles to balance computation, communication and I/O. In addition, PARAS has offline tools to facilitate cross program development, algorithm prototyping and **load** balancing. (4 Refs)

11/7/61   (Item 9 from file: 2)
DIALOG(R)File   2:INSPEC
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03863414   INSPEC Abstract Number: C91031278
 Title: **Harnessing supercomputers for computational underwater acoustics**
   Author(s): Schultz, M.H.
   Author Affiliation: Dept. of Comput. Sci., Yale Univ., New Haven, CT, USA
   Conference Title: Computational Acoustics. Proceedings of the 2nd IMACS Symposium   p.239-42 vol.1
   Editor(s): Lee, D.; Cakmak, A.; Vichnevetsky, R.
   Publisher: North-Holland, Amsterdam, Netherlands
   Publication Date: 1990 Country of Publication: Netherlands   3 vol. (x+276+x+322+x+343) pp.
   ISBN: 0 444 88723 7
   Conference Sponsor: IMACS; Office Naval Res.; Princeton Univ.; Naval Underwater Syst. Center
   Conference Date: 15-17 March 1989   Conference Location: Princeton, NJ, USA
   Language: English   Document Type: Conference Paper (PA)
   Treatment: General, Review (G)
   Abstract: In the context of computational underwater acoustics, there are two distinct regimes: (1) the high end, which will be handled by massively parallel supercomputers. This is basically the 'numerical ocean basin' which will allow one to study new acoustic phenomena and to validate approximate models; (2) the low end, which will be handled by parallel workstations. This is basically a vehicle for code development, computations using the inexpensive approximate models validate on the high end machine, and **visualization** of the results of the computations. Two emerging technologies can be used to tackle the problems: massively parallel computers and reduced instruction set computers (RISC) which will form the **nodes** of parallel machines. There are a large number of innovative parallel architectures being developed by a large number of companies. From the present point of view, probably the most interesting in the long run will be the multicomputers essentially composed of computers with their own distinct private memories with some sort of high **performance** interconnect scheme. Such systems not only provide the potential for very large amounts of CPU power but are an excellent way of providing very large amounts of memory with a very large aggregate bandwidth. (3 Refs)

11/7/62   (Item 10 from file: 2)

03067813   INSPEC Abstract Number: C88012849
 Title: Distributed simulation using Petri nets
  Author(s): Tamer Ozsu, M.
  Author Affiliation: Dept. of Comput. Sci., Alberta Univ., Edmonton, Alta., Canada
  Conference Title: Proceedings of the 1987 Summer Computer Simulation Conference   p.3-8
  Editor(s): Chou, J.Q.B.
  Publisher: SCS, San Diego, CA, USA
  Publication Date: 1987 Country of Publication: USA   xliv+1021 pp.
  ISBN: 0 911801 20 0
  Conference Sponsor: SCS
  Conference Date: 27-30 July 1987   Conference Location: Montreal, Que., Canada
  Language: English   Document Type: Conference Paper (PA)
  Treatment: Practical (P)

  Abstract: One of the problems of traditional simulation techniques is the computational cost of running the simulation experiments. With the advances in distributed computing, distributed simulation has started to emerge as a viable alternative for reducing the computational time of simulations. The authors reports on a distributed simulation methodology that is based on the simulation of Petri nets, C. Petri (1968). It requires that each model be represented as a graph (or a net) which can consist of various subnets. Thus, the models are modular by definition, making them amenable for distributed simulation. The simulation methodology provides the primitives by which subnets in the model can 'communicate' with one another, thus facilitating the distribution of model subnets to various computing **nodes**
. (22 Refs)

 11/7/63   (Item 1 from file: 6)

1936162 NTIS Accession Number: N96-15971/0
   Visualization **of Unsteady Computational Fluid Dynamics**
   (Final Technical Report, 1 Jan. - 31 Dec. 1995)
   Massachusetts Inst. of Tech., Cambridge.
   Corp. Source Codes: 001450000; MJ700802
   Sponsor: National Aeronautics and Space Administration, Washington, DC.
   Report No.: NAS 1.26:199399; NASA-CR-199399
   Oct 95   16p
   Languages: English
   Journal Announcement: GRAI9608; STAR3403
   Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
   NTIS Prices: PC A03/MF A01
   Country of Publication: United States
   Contract No.: NAG2-884
   The current computing environment that most researchers are using for the calculation of 3D unsteady Computational Fluid Dynamic (CFD) results is a super-computer class machine. The Massively **Parallel Processors** (**MPP 's**) such as the 160 **node** IBM SP2 at NAS and clusters of workstations acting as a single **MPP** (like NAS's SGI Power-Challenge array) provide the required computation bandwidth for CFD calculations of transient problems. Work is in progress on a set of software tools designed specifically to address visualizing 3D unsteady CFD results in these super-computer-like

environments. The **visualization** is concurrently executed with the CFD solver. The parallel version of Visual3, pV3 required splitting up the unsteady **visualization** task to allow execution across a network of workstation(s) and compute servers. In this computing model, the network is almost always the **bottleneck** so much of the effort involved techniques to reduce the size of the data transferred between machines.

11/7/64   (Item 2 from file: 6)
DIALOG(R)File   6:NTIS
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1922376   NTIS Accession Number: AD-A253 712/4
  STRIDE   Towards   Practical   3 - D Device   Simulation--Numerical and Visualization   **Considerations.   (Reannouncement   with   New   Availability Information)**
  Wu, K. C. ; Chin, G. R. ; Dutton, R. W.
  Stanford Univ., CA. Dept. of Electrical Engineering.
  Corp. Source Codes: 009225022; 400852
  Sponsor: Army Research Office, Research Triangle Park, NC.
  Report No.: ARO-28297.4-EL
  Sep 91   10p
  Languages: English   Document Type: Journal article
  Journal Announcement: GRAI9604
  Pub. in IEEE Transactions on Computer-Aided Design, v10 n9 p1132-1140, Sep 91. Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers);   (703)605-6000   (other   countries);   fax   at   (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
  NTIS Prices: PC A02/MF A01
  Country of Publication: United States
  Contract No.: DAAL03-91-G-0152
  A 3D device solver (STRIDE), capable of solving grids up to 250,000 **nodes** , has been developed on a message-passing multiprocessor. By the use of iterative matrix solvers and Gummel style nonlinear iteration schemes, user memory per **node** is reduced over use of direct solvers and Newton schemes. By using an independent-edge-grouping scheme to increase the vector length to the order of the number of variables, the **vector processing** efficiency is significantly increased without additional floating point operations. We extend the modified-singular-perturbation (MSP) scheme to two-carrier simulations. This significantly speeds up the convergence rate of Gummel style nonlinear iterations. Physical insight gained from the MSP schemes also leads to an automatic switching scheme between various nonlinear schemes based on the monitoring of certain matrix parameters. This allows the incorporation of a previously proposed Newton-1C scheme which offers the best CPU **performance** for normal bipolar simulations. When combined with current convergence criterion, a set of MSP inspired convergence criterion are better able to recognize a practically converged solution. A novel global convergence scheme is also developed based on insight from MSP principles. Interactive user interface and links to graphics tools are provided to support the tool integration efforts. Application of STRIDE is demonstrated by an analysis of latchup trigger current dependence on layout arrangement, TCAD, Device Simulation, Parallel Iteractive Solver, Staggered Nonlinear Algorithms, CMOS Latchup.

11/7/65   (Item 1 from file: 144)
DIALOG(R)File 144:Pascal
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  12880797   PASCAL No.: 97-0143510
  Accurate performance **prediction for massively parallel systems and its**

applications
 Euro-Par'96 : parallel   processing : **Lyon, August 26-29, 1996**
  SIMON J; WIERUM J M
  BOUGE Luc, ed; FRAIGNIAUD Pierre, ed; MIGNOTTE Anne, ed; ROBERT Yves, ed
  Paderborn Center for Parallel Computing -PC SUP 2 Fuerstenallee 11, 33095
Paderborn, Germany
  International Euro-Par conference, 2 (Lyon FRA) 1996-08-26
  Journal: Lecture notes in computer science, **1996** , 1123 1509-1522
  ISSN: 0302-9743 Availability: INIST-16343; 354000063994311970
  No. of Refs.: 16 ref.
  Document Type: P (Serial); C (Conference Proceedings) ; A (Analytic)
  Country of Publication: Germany; United States
  Language: English
  A **performance** prediction method is presented, which accurately predicts
the expected program **execution**   time on massively parallel systems. We
consider distributed-memory architectures with SMD **nodes**   and a fast
communication network. The method is based on a relaxed task graph model, a
queuing model, and a memory hierarchy model. The relaxed task **graph** is a
compact **representation** of communicating processes of an application
mapped onto the target machine. Simultaneous accesses to the **resources** of
a multi-processor **node** are modeled by a queuing network. The **execution**
 time of the application is computed by an evaluation algorithm. An
example application implemented on a massively parallel computer
demonstrates the high accuracy of our model. Furthermore, two applications
of our accurate prediction method are presented.

 11/7/66   (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

05756683   Genuine Article#: WW129   Number of References: 19
Title: A shortest-path routing algorithm for incomplete WK-recursive
   networks
Author(s): Su MY (REPRINT) ; Chen GH; Duh DR
Corporate Source: NATL TAIWAN UNIV,DEPT COMP SCI & INFORMAT ENGN/TAIPEI
   10764//TAIWAN/ (REPRINT); NATL CHI NAN UNIV,DEPT COMP SCI & INFORMAT
   ENGN/TAIPEI//TAIWAN/
Journal: IEEE TRANSACTIONS ON PARALLEL AND DISTRIBUTED SYSTEMS, **1997** , V8
, N4 (APR), P367-379
ISSN: 1045-9219   Publication date: 19970400
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST,
   NEW YORK, NY 10017-2394
Language: English   Document Type: ARTICLE
Abstract: The WK-recursive networks own two structural advantages:
   expansibility and equal degree. A network is expansible if no changes
   to **node** configuration and link connection are necessary when it is
   expanded, and of equal degree ii its **nodes** have the same degree no
   matter what the size is. However, the number oi **nodes** contained in a
   WK-recursive network is restricted to d(t) where d > 1 is the size of
   the basic building block and t greater than or equal to 1 is the level
   of expansion. The incomplete WK-recursive networks, which were proposed
   to relieve this restriction, are allowed to contain an arbitrary number
   of basic building blocks, while preserving the advantages of the
   WK-recursive networks.

      Designing shortest-path routing algorithms ion incomplete networks
   is in general more difficult than for complete networks. The reason is
   that most incomplete networks lack a unified representation. One of the
   contributions of this paper is to demonstrate a useful **representation**

, i.e., the multistage **graph**   **representation** , for the incomplete
WK-recursive networks. On the basis of it, a shortest-path routing
algorithm is then proposed. With O(d . t) time preprocessing, this
algorithm lakes O(t) time for each intermediate **node** to determine the
next **node** along the shortest path.

11/7/67   (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
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05480666   Genuine Article#: WB610   Number of References: 19
Title: **PARALLEL STEREOCORRELATION ON A RECONFIGURABLE MULTIRING NETWORK**
Author(s): ARABNIA HR; BHANDARKAR SM
Corporate Source: UNIV GEORGIA,DEPT COMP SCI,BOYD GRAD STUDIES RES CTR
    415/ATHENS//GA/30602
Journal: JOURNAL OF SUPERCOMPUTING, **1996** , V10, N3, P243-269
ISSN: 0920-8542
Language: ENGLISH   Document Type: ARTICLE
Abstract: A reconfigurable network termed as the reconfigurable multi-ring
    network (RMRN) is described. The RMRN is shown to be a truly scalable
    network in that each **node** in the network has a fixed degree of
    connectivity and the reconfiguration mechanism ensures a network
    diameter of O(log(2) N) for an N-processor network. Algorithms for the
    two-dimensional mesh and the SIMD or SPMD n-cube are shown to map very
    elegantly onto the RMRN. Basic message passing and reconfiguration
    primitives for the SIMD/SPMD RMRN are designed for use as building
    blocks for more complex parallel algorithms. The RMRN is shown to be a
    viable architecture for image processing and computer vision problems
    using the parallel computation of the stereocorrelation imaging
    operation as an example. Stereocorrelation is one of the most
    computationally intensive imaging tasks. It is used as a **visualization**
     tool in many applications, including remote sensing, geographic
    information systems and robot vision.

11/7/68   (Item 3 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
(c) 2000 Inst for Sci Info. All rts. reserv.

03955144   Genuine Article#: QV520   Number of References: 31
Title: **A PARALLEL ALGORITHM FOR COMPUTING POLYGON SET OPERATIONS**
Author(s): KARINTHI R; SRINIVAS K; ALMASI G
Corporate Source: W VIRGINIA UNIV,CONCURRENT ENGN RES
    CTR/MORGANTOWN//WV/26506; W VIRGINIA UNIV,DEPT COMP
    SCI/MORGANTOWN//WV/26506
Journal: JOURNAL OF PARALLEL AND DISTRIBUTED COMPUTING, **1995** , V26, N1 (
    APR 1), P85-98
ISSN: 0743-7315
Language: ENGLISH   Document Type: ARTICLE
Abstract: We present a parallel algorithm for performing boolean set
    operations on generalized polygons that have holes in them. The
    intersection algorithm has a processor complexity of O(m(2)n(2))
    processors and a time complexity of O(max(2log m, log(2) n)), where m
    is the maximum number of **vertices** in any loop of a polygon, and n is
    the maximum number of loops per polygon. The union and difference
    algorithms have a processor complexity of O(m(2)n(2)) and time
    complexity of O(log m) and O(2log m, log n) respectively. The algorithm
    is based on the EREW PRAM model. The algorithm tries to minimize the
    intersection point computations by intersecting only a subset of loops
    of the polygons, taking advantage of the topological structure of the
    two polygons. We believe this will result in better **performance** on

the average as compared to the worst case. Though all the algorithms presented here are deterministic, randomized algorithms such as sample sort can be used for the sorting subcomponent of the algorithms to obtain fast practical implementations. (C) 1995 Academic Press, Inc.

11/7/69   (Item 1 from file: 62)
DIALOG(R)File   62:SPIN(R)
(c) 2000 American Institute of Physics. All rts. reserv.

00592827
  Application of MPP **to particle tracking**
  Bourianoff, George; Cole, Ben; Chang, Long
  SSC Laboratory, Dallas, Texas 75237
  AIP Conf. Proc.; 297(1),19-26 (25 DEC. 1993)   CODEN: APCPC
  CPM: 9402-I-0339
  Conference Title: Computational accelerator physics
  Conference Location: Los Alamos, New Mexico (USA)
  Conference Year: 22-26 Feb 1993
  Work Type: COMPUTING Document Type: CONFERENCE PAPER
    The SSC requires massive simulation to support the design, commissioning, and operation of the accelerator complex. To this end, the laboratory has made a significant commitment to **MPP** for this application.
    A 64 **node** IPSC/860 was acquired in January of 1991 and has been used extensively in tracking studies of various accelerators of the SSC injector chain. This talk will detail the accomplishments to date and lessons learned. The most basic observation one can make about tracking on a parallel computer is that for a thin element kick code in the absence of space charge, the problem has a natural granularity that makes it ''embarrassingly parallel.'' One simply distributes the particles over available **nodes** and tracks.   No intermode communication is required except for a small amount of diagnostic information that is generated as the run progresses. Hence, the parallel efficiency approaches 100 percent and the problem is scalable to a large number of processors. This seemingly trivial observation leads immediately to two important conclusions regarding the hardware configuration used to do the tracking. The number of computational **nodes** should not exceed the number of particles tracked and the overall **performance** of the calculation will be dominated by single **node** **performance** . The situation becomes less clear as more intermode communication is added. The **performance** of the **MPP** system on runs where beam emittance is monitored or beam instrumentation is simulated are progressively influenced by message passing overhead. In general, one must be aware that it is sometimes better to abandon the natural granularity and compromise network **performance** in the interests of optimizing individual **node** **performance** . The addition of space charge forces to the tracking code requires a PIC calculation to be done concurrently with the thin element tracking. A procedure for dynamically sorting particles on to **nodes** that optimizes machine **performance** will be described.   The application of a **MPP** to serve as the engine of real time simulator will be discussed.   Such factors as predictability of network collisions and the interrupt response time of the individual **node** required to write out data becomes important. An interactive **visualization** system designed to display the results from the space charge calculation will be described. It has great flexibility in choice of viewpoint, reference frame and data density.
?

```
?show files;ds
File 624:McGraw-Hill Publications 1985-2000/May 04
         (c) 2000 McGraw-Hill Co. Inc
File 621:Gale Group New Prod.Annou.(R) 1985-2000/May 10
         (c) 2000 The Gale Group
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         (c) 2000 The Gale Group
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         (c) 2000 The Gale Group
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         (c) 2000 Bell & Howell
File 813:PR Newswire 1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc
File 613:PR Newswire 1999-2000/May 10
         (c) 2000 PR Newswire Association Inc
File  16:Gale Group PROMT(R) 1990-2000/May 10
         (c) 2000 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 141:Readers Guide 1983-2000/Dec
         (c) 2000 The HW Wilson Co
File 370:Science 1996-1999/Jul W3
         (c) 1999 AAAS
File 696:DIALOG Telecom. Newsletters 1995-2000/May 09
         (c) 2000 The Dialog Corp.
File 148:Gale Group Trade & Industry DB 1976-2000/May 10
         (c)2000 The Gale Group
File 553:Wilson Bus. Abs. FullText 1982-1999/Sep
         (c) 1999 The HW Wilson Co


Set     Items   Description
S1      46005   (PARALLEL OR PIPELINE OR ARRAY OR VECTOR OR CONCURRENT? OR
                SIMULTANEOUS?)(2N)(PROCESSOR? ? OR PROCESSING OR SERVER)
S2      20493   HYPERCUBE? ? OR HYPER()CUBE? ? OR SMP OR MPP
S3    7261429   CAPACITY OR PERFORMANCE OR LOAD OR EXECUT?(2N)TIME? ? OR R-
                ESOURCE? ? OR THROUGHPUT OR THROUGH()PUT OR TRAFFIC OR CONCUR-
                RENCY OR BOTTLENECK? ? OR TRACE()TOOL? ? OR STATISTIC? ? OR W-
                ORKLOAD OR CLUSTER(2N)MANAG? OR DATA()HANDLING
S4    2898652   GRAPH? OR VISUAL? OR PICTORIAL OR PICTURE OR 3()D OR THREE-
                ()DIMENSIONAL OR 3D OR IMAGE OR IMAGES OR ILLUSTRATION OR X()Y
                OR XY OR MATRIX OR MATRICES
S5     424328   NODE OR NODES OR VERTEX OR VERTICES OR CORNER OR TRIANGULAR
                OR TRIANGLE? ? OR CROSS()POINT? ? OR CROSSPOINT? ? OR FORK? ?
S6       2719   (S1 OR S2) AND S3 AND S4 AND S5
S7        237   (S1 OR S2)(S)S3(S)S4(S)S5
S8      50624   S4(5N)(REPRESENTATION OR VISUALIZATION OR VISUALISATION)
S9        313   (S1 OR S2) AND S3 AND S5 AND S8
S10       230   S9 AND PY<1998
S11       176   RD (unique items)
S12        10   (S1 OR S2)(S)S3(S)S5(S)S8
S13        10   S12 AND PY<1998
S14         6   RD (unique items)
?
```

1 May 10, 2000 11:24

?t14/3,k/all

14/3,K/1   (Item 1 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
(c) 2000 The Gale Group. All rts. reserv.

03487204   Supplier Number: 47190601   (USE FORMAT 7 FOR FULLTEXT)
**SUN MOVES IN ON THE HIGH PERFORMANCE COMPUTING MARKET WITH THE ULTRA HPC
 SERVER LINE**
Computergram International, n3115, pN/A
March 7, 1997
Language: English   Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 572

   (USE FORMAT 7 FOR FULLTEXT)
TEXT:
...CI No 3,021), Sun Microsystems Inc is pursuing Silicon Graphics Inc and
other high-**performance** computing players by bundling its Ultra Enterprise
 SMP symmetric multi-processing servers with a raft of parallelising
software, development tools and applications and...

...machines, Sun will sell and support version 2.2 of Platform Computing
Corp's popular **Load** Sharing Facility software for monitoring and managing
 resources , plus Fortran77, Fortran90, multi-threading development and
debugging tools. By year-end it will introduce...
...it acquired from Thinking Machines Corp, in the form of the Prism
parallel debugging and **visualisation** tools. At least some of the
clustering options will be provided by Sun's forthcoming...

...GlobalWorks will enable developers to address a cluster of systems as a
single virtual processing **node** . The 1Gbps SCI Sbus adaptor boards being
created for clustering Sun servers by Dolphin Interconnect...

...At the same time, Solaris is scheduled to support 64-bit virtual address
space and **cluster** system **management** plus the **cluster** file system
required to allow users to write their own clustered applications. The
servers start...
19970307

14/3,K/2   (Item 2 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
(c) 2000 The Gale Group. All rts. reserv.

01474841   Supplier Number: 42030110   (USE FORMAT 7 FOR FULLTEXT)
PARALLEL COMPUTING APPLICATIONS GROUP
Computergram International, n1661, pN/A
April 26, 1991
Language: English   Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 116

   (USE FORMAT 7 FOR FULLTEXT)
TEXT:
...of Trade and Industry, to develop parallel computing applications for a
computer architecture designed by **parallel   processing** specialist Caplin
Cybernetics, built around the new Inmos T9000 Transputer: the goal of the
project...

...limitations of existing parallel machines; the system will be designed
to offer peak floating-point **performance** of 100 MFLOPS per **node** ;

planned applications for the general-purpose system include oil reservoir simulation, **three -dimensional   visualisation** and neural network modelling.
 19910426

 14/3,K/3   (Item 3 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
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01332127   Supplier Number: 41571416   (USE FORMAT 7 FOR FULLTEXT)
STARDENT LAUNCHES STILETTO DESKTOPS, ADDS 3000VS MODELS
Computergram International, n1520, pN/A
Sept 27, 1990
Language: English   Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 421

   (USE FORMAT 7 FOR FULLTEXT)
TEXT:
...R3000 RISC chip, each with a tightly-coupled Intel 80860 RISC part acting as a **vector** co-**processor** . Each processor is rated by Stardent at 32 MIPS and 48 MFLOPS giving an overall **performance** of 64 MIPS and 96 MFLOPS. They run version 3 of the Application **Visualisation** System **graphics** subsystem from the Stellar side of the company - this uses two 80860s for three-dimensional...

...claimed to perform 190,000 three-dimensional vectors, and 40,000 100-pixel gouraud-shaded **triangles** operations per second. Running a version of AT&T's Unix V.3 and the...
...what it describes as the "world's first medical imaging supercomputer." The Stardent 3000VS Series **Visualisation** Systems are essentially the Ardent-based 3000 systems running Stellar's VX graphics subsystem, using...

...32MHz MIPS R3000 part, available in one to four processor configurations, offering a top-end **performance** of 128 MFLOPS going from $100,000 to $300,000. They are available as upgrades...
 19900927

 14/3,K/4   (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2000 The Gale Group. All rts. reserv.

06197493   SUPPLIER NUMBER: 13438654   (USE FORMAT 7 OR 9 FOR FULL TEXT)
**Unparalleled Processing. (Thinking Machines' CM-5 Scale 3
 supercomputer)(Product Spotlight) (Product Announcement)**
Belleville, Laureen
Computer Graphics World, v15, n12, p18(1)
Dec, 1992
DOCUMENT TYPE: Product Announcement   ISSN: 0271-4159   LANGUAGE:
   ENGLISH   RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 467   LINE COUNT: 00036

...ABSTRACT: its $750,000 Connection Machine 5 Scale 3, a scalable supercomputer that combines peak processing **capacity** of up to 4GFLOPS, the CMOST Unix operating system and integrated multiGbytes of file storage. The CM 5 Scale 3 also features multiple 9.6Gbyte disk storage **nodes** , up to 32 of Thinking Machines' 128MFLOPS **parallel   processing   nodes** and the full set of Connection Machine software. CM 5 Scale 3 is the company...

...to the company because such machines fit into the smaller configurations

where most of the **parallel   processing** potential is located. Thinking
Machines also introduces its first fully integrated version of the
Application **Visualization** System, the CM AVS. Intended for parallel
computers, CM AVS enables users to interactively visualize...

19921200

14/3,K/5   (Item 2 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2000 The Gale Group. All rts. reserv.

05419769   SUPPLIER NUMBER: 11076251   (USE FORMAT 7 OR 9 FOR FULL TEXT)
**IBM RISC announcements: enhances RISC System/6000 graphics, disk storage:
 announces innovative visualization system. (reduced instruction set
 computers) (product announcement)**
EDGE: Work-Group Computing Report, v2, n62, p41(1)
July 29, 1991
DOCUMENT TYPE: product announcement   LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT
WORD COUNT: 1416   LINE COUNT: 00117

...   Design/Computer Aided Manufacturing. It has a planned availability
of October 25. o IBM POWER **Visualization** System: This total solution for
scientific **visualization** combines advanced hardware, an integrated user
environment optimized for **visualization** , and the latest in communications
and storage technology to give scientists a new tool for their most
challenging projects. Users access the power of the **visualization** system
through a RISC System/6000 that functions as a **visualization** workstation.
Planned availability is November 22, with prices ranging from $600,000 to
$2 million depending on options selected. Elements of the system include: -
the IBM POWER **Visualization** Server with up to 32 **parallel   processors**
that features the Data Explorer integrated **visualization** environment,
which supports industry-standard X Window System and OSF/Motif interfaces -
a dedicated RISC...

...the optional IBM Disk Array Subsystem for holding the large amounts of
data needed for **visualization** projects. This storage method, with a
capacity of up to 170 gigabytes, speeds large blocks of data to the
visualization server at a faster rate than conventional high-**performance**
disk storage units. - the optional IBM POWER **Visualization** Video
Controller, attached to the **visualization** workstation, which allows
high-resolution **images** generated by the IBM POWER **Visualization** Server
to be displayed at the workstation. This enables support for
High-Definition Television (HDTV) displays. - High **Performance** Parallel
Interface (HIPPI) networking capability, which allows data to be
transferred among the **visualization   server** , disk **array** and video
controller five to 10 times faster than conventional workstation network
channels. HIPPI also permits the **visualization** system to connect to
supercomputers and mainframe computers. o IBM AIX **Visualization** Data
Explorer/6000: This application software product allows a user to perform
advanced **visualization** on a standalone RISC System/6000 workstation. Its
flexible design allows both novice and expert...

...render data through a rich set of functions compatible with those on the
IBM POWER **Visualization** System. Planned availability is December 20, with
a price of $5,900. o 9333 High-**Performance** Disk Drive Subsystem: This
product comes in two models -- one a deskside unit that attaches...

...POWERserver 9XX systems. Both models feature a new Serial-Link
connection capability to deliver improved **performance** .
     Up to four subsystems can be attached via a single adapter to provide

a total...

19910729

14/3,K/6   (Item 3 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

05136953   SUPPLIER NUMBER: 10640664   (USE FORMAT 7 OR 9 FOR FULL TEXT)
Minigrams.
Computergram International, n1561, CGI04260015
April 26, 1991
ISSN: 0268-716X   LANGUAGE: ENGLISH   RECORD TYPE: FULLTEXT
WORD COUNT: 2513   LINE COUNT: 00211

...   of Trade and Industry, to develop parallel computing applications
for a computer architecture designed by **parallel   processing** specialist
Caplin Cybernetics, built around the new Inmos T9000 Transputer: the goal
of the project...

...limitations of existing parallel machines; the system will be designed
to offer peak floating-point **performance** of 100 MFLOPS per **node** ;
planned applications for the general-purpose system include oil reservoir
simulation, **three -dimensional   visualisation** and neural network
modelling.
     - o -
     Interactive Systems Corp, whose appointment as principal publisher of
Unix...

19910426
?

```
?show files;ds
File  15:ABI/INFORM(R) 1971-2000/May 08
         (c) 2000 Bell & Howell
File  88:Gale Group Business A.R.T.S. 1976-2000/May 10
         (c) 2000 The Gale Group
File   9:Business & Industry(R) Jul/1994-2000/May 10
         (c) 2000 Resp. DB Svcs.
File  13:BAMP 2000/Apr W5
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File 623:Business Week 1985-2000/Apr W5
         (c) 2000 The McGraw-Hill Companies Inc
File 810:Business Wire 1986-1999/Feb 28
         (c) 1999 Business Wire
File 610:Business Wire 1999-2000/May 10
         (c) 2000 Business Wire.
File 647:CMP  Computer Fulltext 1988-2000/Apr W5
         (c) 2000 CMP
File 275:Gale Group Computer DB(TM) 1983-2000/May 10
         (c) 2000 The Gale Group
File 674:Computer News Fulltext 1989-2000/Mar W2
         (c) 2000 IDG Communications
File  98:General Sci Abs/Full-Text 1984-1999/Oct
         (c) 1999 The HW Wilson Co.
File  47:Gale Group Magazine DB(TM) 1959-2000/May 10
         (c) 2000 The Gale group
File  75:TGG Management Contents(R) 86-2000/Apr W5
         (c) 2000 The Gale Group
File 239:Mathsci 1940-2000/Jun
         (c) 2000 American Mathematical Society
```

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Set     Items    Description
S1      38027    (PARALLEL OR PIPELINE OR ARRAY OR VECTOR OR CONCURRENT? OR
                 SIMULTANEOUS?)(2N)(PROCESSOR? ? OR PROCESSING OR SERVER)
S2      15005    HYPERCUBE? ? OR HYPER()CUBE? ? OR SMP OR MPP
S3    3127669    CAPACITY OR PERFORMANCE OR LOAD OR EXECUT?(2N)TIME? ? OR R-
                 ESOURCE? ? OR THROUGHPUT OR THROUGH()PUT OR TRAFFIC OR CONCUR-
                 RENCY OR BOTTLENECK? ? OR TRACE()TOOL? ? OR STATISTIC? ? OR W-
                 ORKLOAD OR CLUSTER(2N)MANAG? OR DATA()HANDLING
S4    2265452    GRAPH? OR VISUAL? OR PICTORIAL OR PICTURE OR 3()D OR THREE-
                 ()DIMENSIONAL OR 3D OR IMAGE OR IMAGES OR ILLUSTRATION OR X()Y
                 OR XY OR MATRIX OR MATRICES
S5     335161    NODE OR NODES OR VERTEX OR VERTICES OR CORNER OR TRIANGULAR
                 OR TRIANGLE? ? OR CROSS()POINT? ? OR CROSSPOINT? ? OR FORK? ?
S6       3059    (S1 OR S2) AND S3 AND S4 AND S5
S7        182    (S1 OR S2)(S)S3(S)S4(S)S5
S8      38068    S4(5N)(REPRESENTATION OR VISUALIZATION OR VISUALISATION)
S9        408    (S1 OR S2) AND S3 AND S5 AND S8
S10       353    S9 AND PY<1998
S11       225    RD (unique items)
S12        10    (S1 OR S2)(S)S3(S)S5(S)S8
S13         9    S12 AND PY<1998
S14         9    RD (unique items)
?t14/3,k/all
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 14/3,K/1   (Item 1 from file: 15)
DIALOG(R)File 15:ABI/INFORM(R)
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01222933 98-72328
Powerful on-campus computing for industry
Falcao, Djalma M
IEEE Spectrum v33n6 PP: 32 Jun 1996

ISSN: 0018-9235 JRNL CODE: SPC

ABSTRACT: The Laboratory for High-**Performance** Computing at the Federal
University of Rio de Janeiro's Graduate School of Engineering focuses...

... joint projects with the lab. The lab owns 3 different state-of-the-art
high- **performance**   parallel computers: an 8- **node** Intel iPSC/860
 hypercube   computer, an 8-processor Cray J90, and a 4-processor IBM SP2
system,   as   well   as   SunSparc20   workstations   for **graphics**   and
 visualization .

 14/3,K/2   **(Item 1 from file: 9)**
DIALOG(R)File   9:Business & Industry(R)
(c) 2000 Resp. DB Svcs. All rts. reserv.

01467521 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Silicon Graphics Intros Data Warehouse Mining Tools
(Silicon Graphics unveils MineSet data analysis and mining tools, and
 Challenger DataArray, chain of supporting SGI servers)
Newsbytes News Network, p N/A
April 16, 1996
DOCUMENT TYPE: Journal (United States)
LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 509

ABSTRACT:
...is based around the concept of a software backplane which will support
data mining and **visualization** ·plug-in tools from SGI and independent
software vendors. The Challenge DataArray server cluster can be configured
from two to eight Challenge **nodes** with each **node** supporting one to
thirty-six MIPS RISC R4400 or R10000 processors, for a maximum of 288
processors . The **array** also supports up to 128 gigabytes (GB) of system
memory and 288 fast and wide...

...38 terabytes non-RAID (redundant array of inexpensive disks) and 125
terabytes of RAID disk **capacity** is possible with the Challenge Data
Array. Shipment is expected in the first half of...

 14/3,K/3   **(Item 1 from file: 275)**
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2000 The Gale Group. All rts. reserv.

02042919   SUPPLIER NUMBER: 19185199   (USE FORMAT 7 OR 9 FOR FULL TEXT)
SUN MOVES IN ON THE HIGH PERFORMANCE COMPUTING MARKET WITH THE ULTRA HPC
 SERVER LINE.
Computergram International, n3115, pCGN03070007
March 7, 1997
ISSN: 0268-716X   LANGUAGE: English   RECORD TYPE: Fulltext
WORD COUNT: 608   LINE COUNT: 00052

TEXT:
     ...CI No 3,021), Sun Microsystems Inc is pursuing Silicon Graphics Inc
and other high-**performance** computing players by bundling its Ultra
Enterprise **SMP** symmetric multi-processing servers with a raft of
parallelising software, development tools and applications and...

...machines, Sun will sell and support version 2.2 of Platform Computing
Corp's popular **Load** Sharing Facility software for monitoring and managing
 resources , plus Fortran77, Fortran90, multi-threading development and
debugging tools. By year-end it will introduce...

...it acquired from Thinking Machines Corp, in the form of the Prism
parallel debugging and **visualisation** tools. At least some of the
clustering options will be provided by Sun's forthcoming...

...GlobalWorks will enable developers to address a cluster of systems as a
single virtual processing **node** . The 1Gbps SCI Sbus adaptor boards being
created for clustering Sun servers by Dolphin Interconnect...

...At the same time, Solaris is scheduled to support 64-bit virtual address
space and **cluster** system **management** plus the **cluster** file system
required to allow users to write their own clustered applications. The
servers start...

19970307

14/3,K/4   (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2000 The Gale Group. All rts. reserv.

01553747   SUPPLIER NUMBER: 13438654   (USE FORMAT 7 OR 9 FOR FULL TEXT)
Unparalleled Processing. (Thinking Machines' CM-5 Scale 3
 supercomputer)(Product Spotlight) (Product Announcement)
Belleville, Laureen
Computer Graphics World, v15, n12, p18(1)
Dec, 1992
DOCUMENT TYPE: Product Announcement   ISSN: 0271-4159   LANGUAGE:
   ENGLISH   RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 467   LINE COUNT: 00036

...ABSTRACT: its $750,000 Connection Machine 5 Scale 3, a scalable
supercomputer that combines peak processing **capacity** of up to 4GFLOPS,
the CMOST Unix operating system and integrated multiGbytes of file storage.
The CM 5 Scale 3 also features multiple 9.6Gbyte disk storage **nodes** , up
to 32 of Thinking Machines' 128MFLOPS **parallel   processing   nodes** and
the full set of Connection Machine software. CM 5 Scale 3 is the company...

...to the company because such machines fit into the smaller configurations
where most of the **parallel   processing** potential is located. Thinking
Machines also introduces its first fully integrated version of the
Application **Visualization** System, the CM AVS. Intended for parallel
computers, CM AVS enables users to interactively visualize...

19921200

14/3,K/5   (Item 3 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2000 The Gale Group. All rts. reserv.

01443317   SUPPLIER NUMBER: 11076251   (USE FORMAT 7 OR 9 FOR FULL TEXT)
IBM RISC announcements: enhances RISC System/6000 graphics, disk storage:
 announces innovative visualization system. (reduced instruction set
 computers) (product announcement)
EDGE: Work-Group Computing Report, v2, n62, p41(1)
July 29, 1991
DOCUMENT TYPE: product announcement   LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT
WORD COUNT: 1416   LINE COUNT: 00117

    ...   Design/Computer Aided Manufacturing. It has a planned availability

3 May 10, 2000 11:12

of October 25. o IBM POWER **Visualization** System: This total solution for scientific **visualization** combines advanced hardware, an integrated user environment optimized for **visualization** , and the latest in communications and storage technology to give scientists a new tool for their most challenging projects. Users access the power of the **visualization** system through a RISC System/6000 that functions as a **visualization** workstation. Planned availability is November 22, with prices ranging from $600,000 to $2 million depending on options selected. Elements of the system include: - the IBM POWER **Visualization** Server with up to 32 **parallel processors** that features the Data Explorer integrated **visualization** environment, which supports industry-standard X Window System and OSF/Motif interfaces - a dedicated RISC...

...the optional IBM Disk Array Subsystem for holding the large amounts of data needed for **visualization** projects. This storage method, with a **capacity** of up to 170 gigabytes, speeds large blocks of data to the **visualization** server at a faster rate than conventional high-**performance** disk storage units. - the optional IBM POWER **Visualization** Video Controller, attached to the **visualization** workstation, which allows high-resolution **images** generated by the IBM POWER **Visualization** Server to be displayed at the workstation. This enables support for High-Definition Television (HDTV) displays. - High **Performance** Parallel Interface (HIPPI) networking capability, which allows data to be transferred among the **visualization** **server** , disk **array** and video controller five to 10 times faster than conventional workstation network channels. HIPPI also permits the **visualization** system to connect to supercomputers and mainframe computers. o IBM AIX **Visualization** Data Explorer/6000: This application software product allows a user to perform advanced **visualization** on a standalone RISC System/6000 workstation. Its flexible design allows both novice and expert...

...render data through a rich set of functions compatible with those on the IBM POWER **Visualization** System. Planned availability is December 20, with a price of $5,900. o 9333 High-**Performance** Disk Drive Subsystem: This product comes in two models -- one a deskside unit that attaches...

...POWERserver 9XX systems. Both models feature a new Serial-Link connection capability to deliver improved **performance** .
     Up to four subsystems can be attached via a single adapter to provide a total...

19910729

14/3,K/6   (Item 4 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01427406   SUPPLIER NUMBER: 10640664   (USE FORMAT 7 OR 9 FOR FULL TEXT)
Minigrams.
Computergram International, n1561, CGI04260015
April 26, 1991
ISSN: 0268-716X   LANGUAGE: ENGLISH   RECORD TYPE: FULLTEXT
WORD COUNT: 2513   LINE COUNT: 00211

...   of Trade and Industry, to develop parallel computing applications for a computer architecture designed by **parallel processing** specialist Caplin Cybernetics, built around the new Inmos T9000 Transputer: the goal of the project...

...limitations of existing parallel machines; the system will be designed to offer peak floating-point **performance** of 100 MFLOPS per **node** ;

planned applications for the general-purpose system include oil reservoir simulation, **three -dimensional   visualisation** and neural network modelling.
          - o -
     Interactive Systems Corp, whose appointment as principal publisher of Unix...

19910426

14/3,K/7   (Item 5 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01371756   SUPPLIER NUMBER: 09461105   (USE FORMAT 7 OR 9 FOR FULL TEXT)
Stardent launches Stiletto desktops, adds 3000VS models. (Stardent Computer Inc.) (product announcement)
Computergram International, n1520, pCGI09570002
Sept 27, 1990
DOCUMENT TYPE: product announcement   ISSN: 0268-716X   LANGUAGE: ENGLISH   RECORD TYPE: FULLTEXT
WORD COUNT: 452   LINE COUNT: 00036

...   R3000 RISC chip, each with a tightly-coupled Intel 80860 RISC part acting as a **vector** co-**processor** . Each processor is rated by Stardent at 32 MIPS and 48 MFLOPS giving an overall **performance** of 64 MIPS and 96 MFLOPS. They run version 3 of the Application **Visualisation** System **graphics** subsystem from the Stellar side of the company - this uses two 80860s for three-dimensional...

...claimed to perform 190,000 three-dimensional vectors, and 40,000 100-pixel gouraud-shaded **triangles** operations per second. Running a version of AT&T's Unix V.3 and the...

...what it describes as the "world's first medical imaging supercomputer." The Stardent 3000VS Series **Visualisation** Systems are essentially the Ardent-based 3000 systems running Stellar's VX graphics subsystem, using...

...32MHz MIPS R3000 part, available in one to four processor configurations, offering a top-end **performance** of 128 MFLOPS going from $100,000 to $300,000. They are available as upgrades...

19900927

14/3,K/8   (Item 1 from file: 674)
DIALOG(R)File 674:Computer News Fulltext
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053293
OLYMPICS
52
www.atlanta.olympics.org
Byline: Joseph Maglitta
Journal: Computerworld   Page Number: 92
Publication Date: July 15, 1996
Word Count: 1008   Line Count: 100

Publication Year: **1996**
Text:
... 7,000 IBM PCs and ThinkPads, 80 AS/400 servers, two RS/6000 SP massively **parallel   processors** APPLICATIONS100 at 30 venues ON-SITE

5 May 10, 2000 11:12

USERS150,000, including: 40,000 volunteers 31...

... employees 15,000 athletes 15,000 members of the media 100 heads of state WEB **TRAFFIC** Before Games: About 250,000 visits daily During Games: More than 6 millionexpected daily...

... to a secure DB2 database on an SP2. INTERNET SERVERSOne RS/6000 SP2 scalable **parallel** **processor** with 52 **nodes** in Southbury, Conn.SECOND SERVEROne RS/6000 SP2 with 16 **nodes** in Hawthorne, N.Y.Each **node** has 250M to 512M bytes of memory and 4G bytes of DASD. Systems have Asynchronous...

...WORKS: Satellite data for 29 square kilometers around the Games gets fed into a 30-**node** SP2 running IBM's **visualization** data explorer. TECHNOLOGY OPERATIONS CENTERMission control. No, you can't surf through here, either...

 14/3,K/9   **(Item 1 from file: 239)**
DIALOG(R)File 239:Mathsci
(c) 2000 American Mathematical Society. All rts. reserv.

  01614179 MR 81b#68043
 Parallel computations in graph theory.
  Arjomandi, Eshrat Reghbati
  Corneil, D. G.
  SIAM J. Comput.
  SIAM Journal on Computing, **1978** , 7, no. 2, 230--237. ISSN: 0097-5397 CODEN: SMJCAT
  Language: English
  Subfile: MR (Mathematical Reviews) AMS
  Abstract Length: LONG (32 lines)
  Reviewer: O'Neil, P. E. (Lexington, Mass.)

  1978 ,
  The authors derive upper and lower **performance** bounds for optimal graph-theoretic algorithms which use identical **processors** in **parallel** . Two models are considered: an unbounded number of **parallel** **processors** , and a number bounded by a constant K. The processors are capable of performing arithmetic...

...the case of unbounded parallelism) as well as comparisons, accessing common memory which contains a **graph** adjacency **representation** as input. Using the fan-in theorem of J. I. Munro and M. Paterson (J...

...lower bounds for serial computability, the authors show that the following tasks have unbounded parallel **performance** lower bounds of Omega (log n): (1) finding connected components in an undirected graph; (2...

...processors to a constant number of transitive closure computations, for which the best known unbounded **parallel** **processing** time is $O(\log\{sup\}2 \ n)$. This establishes an upper bound. In the case...

...T {sub}1/K+L(log K)+2n, where L is the distance of the **node** farthest from the start **node** . In the case of dense graphs, the breadth-first search technique is therefore nearly optimal...
?